June 21, 1982

Memo To: Distribution

From: Karen Meyers

Subject: Contract with General Instrument for Master Component Game Sets and Cartridge ROMS

In Reply Refer to: KLM-1664

At long last the General Instrument 1981/1982 contract has been signed. Attached is a copy for your file. There are some additional copies available in my department, however, we had to send the contract out to be printed because of the thickness, so please do not lose your copies. In addition to the contract as originally signed, there is also a revised Exhibit C.

Please remember that the information contained in this contract is considered "CONFIDENTIAL" and must not be given to anyone outside of Mattel or left out where it could be available for visitors to see.

Distribution:

S. Prodromou
T.Scott
R. Rambeau
H. Barnes
D. Chandler
J. Fairbanks
H. Cohen
C. Lewis
J. Parker (MEL)
P. Lyons (MEL)
J. Bray (MEL)
J. Ballotti
D. Roberts
C. Akop
J. Tannikawa
S. Harris
J. Wilson

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D. CHANDLER

EXHIBIT C

Shipment Schedule: Game Sets and Cartridge Sets (000)

	GAME SETS				CARTRIDGE SETS			
MONTH	Min.	Cum.	Max.	Cum.	Min.	Cum.	Max.	Cum.
981 Nov.	175	175	175	175	1100	1100	1100	1100
Dec.	150	325	175	350	700	1800	950	2050
982 Jan.	125	450	175	525	400	2200	750	2800
Feb.	175	625	200	725	700	2900	1200	4000
Mar.	175	800	225	950	700	3600	1200	5200
Apr.	175	975	225	1175	700	4300	1200	6400
May	175	1150	235	1410	500	4800	1400	7800
June	175	1325	235	1645	500	5300	1700	9500
July	175	1500	230	1875	500	5800	1600	11100
*Aug.	165	1665	230	2105	400	6200	1700	12800
Sept.	170	1835	235	2340	300	6500	2200	15000
Oct.	165	2000	235	2575	300	6800	1800	16800

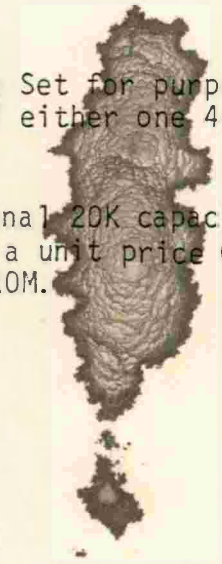
*All Cartridge Set orders scheduled for shipment after August 1, 1982, will be completed with the shipment of one 40K ROM, except as otherwise requested by Buyer.

Note #1: This revision is based upon the following mix of Cartridge Sets:

Month	40K ROMs	20K ROMs
May	150	1250
June	500	1200
July	1200	400
Aug.	1200	500
Sept.	1550	650
Oct.	1300	500

Revision #1
6/8/82

EXHIBIT C



Note 2: A Cartridge Set for purposes of count against Exhibit C, consists of either one 40K ROM or two 20K ROMs.

Note 3: The additional 20K capacity for August through October will be at a unit price of $2.74 per Cartridge Set or $1.37 per ROM.

Revision #1
6/8/82

AGREEMENT OF SALE AND PURCHASE

AGREEMENT made as of the 1st day of November, 1981, by and between GENERAL INSTRUMENT CORPORATION, Microelectronics Division, a Delaware corporation, with a place of business at 600 West John Street, Hicksville, New York ("Seller") and MATTEL, INC., Mattel Electronics Division, a Delaware corporation, with a place of business at 5150 Rosecrans Avenue, Hawthorne, California ("Buyer").

W I T N E S S E T H:

WHEREAS, Seller desires to manufacture and sell certain microelectronic equipment (the "Products") to Buyer and Buyer desires to purchase the Products from Seller;

WHEREAS, Seller and Buyer desire to establish the terms and conditions of sale and purchase for the Products;

NOW, THEREFORE, in consideration of the premises and mutual covenants and agreements set forth herein, the parties agree as follows:

1. Formation of Contract.

Any term or condition of (a) Buyer's purchase order; (b) releases pertaining thereto; (c) Seller's order acknowledgment; or (d) any communication between Buyer and Seller which is in any way inconsistent with the terms and conditions set forth herein shall be deemed to be null and void and shall not be binding on either party hereto, unless agreed to in writing in accordance with the provisions of Paragraph 27.

2. Products.

(a) The Products purchased and sold hereunder shall be those set forth in Exhibit A. The terms "Game Sets" and "Cartridge Sets" shall have the meaning assigned them in Exhibit A. The parties may increase, decrease or modify the items included in the Products at any time by writing in accordance with the provisions of Paragraph 27.

(b) The Products shall be manufactured and shall perform in accordance with the specifications attached to this Agreement as Exhibit B ("Specifications") and Exhibit D ("Quality Requirements").

3. Design Changes.

(a) Buyer may, by written notice, request Seller to provide quotations regarding changes and/or additions (hereinafter referred to as "Design Changes") to the Products, Specifications and Quality Requirements listed in Exhibits A, B and D respectively. Within fourteen (14) business days after receipt of such notice, Seller shall provide Buyer with a written quotation setting forth the design and development costs, production costs and schedule impact for such Design Changes, which quotations shall be valid for a period of thirty (30) days thereafter. In the event the parties agree to implement any such Design Changes, Seller will advise Buyer in writing of the person assigned to accomplish the Design Change, and Seller will provide Buyer with a Design Change plan delineating milestone schedules for implementation of the change. Such Design Changes shall not relieve Buyer of its obligation to accept Products either manufactured prior to

such implementation or reshipped Products returned by Buyer that were found to be in conformance with the Specifications in effect at the time of original shipment of Products or repaired to the Specifications (in lieu of replacement), except that Products returned by Buyer pursuant to Paragraph 8 or 9 hereof more than thirty (30) days after the date of such implementation shall be replaced (if Seller elects to replace) by Products conforming to such Design Changes.

(b) In no event will Seller implement any mask tooling or final test procedure changes to the Products as specified in Exhibits B and G without prior written approval and authorization of Buyer, including the effective date of implementation. The only exception will be those changes in the final test procedures necessitated by (i) the revisions in Exhibit B mutually agreed to by the Seller and Buyer and (ii) the changes in mask tooling and final test procedures envisioned by the program set forth in Paragraph 13(d). Seller will submit qualification samples to Buyer for approval prior to production and delivery of Products affected by such change. Buyer will respond to Seller in writing within four (4) weeks after receipt of any approval request for a mask design tooling change and within two (2) weeks for any approval request for a final test tape change. Buyer shall not unreasonably withhold any such requested approval. Seller will be liable for any cost impact or schedule delay caused by any mask tooling or final test procedure implemented by Seller without prior written approval (or waiver thereof) of Buyer.

4. Tooling.

Seller shall retain title to, possession of, and the right to exclusive use of manufacturing tooling made or obtained by Seller, including all masks, tapes, plots, drawings, fixtures, test programs, equipment and manufacturing aids except as provided in Paragraph 12.

5. Purchase and Sale; Inventory.

(a) In accordance with Exhibit C and subject to subsequent modification thereof as provided herein, Buyer agrees to purchase and Seller agrees to sell the specified minimum cumulative quantity at any given time during the term hereof. Buyer may purchase quantities up to the specified maximum cumulative quantities of Exhibit C, provided such quantities are ordered in accordance with subparagraph (b) below and do not exceed maximum monthly quantities, except as provided in the next sentence. Seller may, at its option, accept purchase quantities in excess of the maximum monthly and/or cumulative quantities specified in Exhibit C. In such event Seller will prepare and forward to Buyer a revised Exhibit C within ten (10) days after acceptance of the subject purchase orders reflecting the greater maximum monthly and/or cumulative quantities, which revised Exhibit C will supersede the prior Exhibit C and will be binding on the parties in accordance with Paragraph 27.

(b) Buyer shall issue purchase orders to Seller identifying the desired quantities of Products at least ninety (90) days prior to the fifteenth day of the subject shipment month for Game Sets and sixty (60) days prior to the fifteenth day of the subject shipment month for Cartridge Sets. The purchase orders

shall refer to this Agreement, describe the Product, specify a delivery date, list the applicable price in accordance with Exhibit A and describe the method of shipment. Seller will acknowledge Buyer's purchase orders within ten (10) days after receipt, which acknowledgment will confirm Seller's obligation to ship Products in accordance with the price, quantity and delivery schedule specified on Buyer's purchase order, provided such price, quantity and delivery schedule are consistent with the terms of this Agreement. Any purchase order which is inconsistent with the terms of this Agreement will be acknowledged by Seller reflecting the terms of this Agreement or, in the case of deliveries, the best delivery schedule available. The price, quantity and delivery set forth in Seller's acknowledgment shall be binding on the Buyer unless Buyer rejects Seller's acknowledgment in writing within three (3) days after receipt thereof.

(c) In addition to the requirements of Exhibit C, commencing in March, 1982 Seller shall maintain a constant inventory of at least twenty thousand (20,000) of each of the Buyer's unique Game Set part numbers (excluding Cartridge Sets) for the purpose of fulfilling Buyer's requirements for spare parts and supplying replacement parts required under Paragraphs 8 and 9. Buyer will issue purchase orders for spare parts on an as required basis. Seller will date code all spare parts as of the date of shipment to Buyer.

6. Packing, Transportation, Title and Risk of Loss.

(a) Seller shall, at its own expense, box, crate, pack and package all the Products in a commercially reasonable manner in

compliance with the requirements of common carriers. Shipments shall be addressed to Buyer (including Buyer's agents) at such address as Buyer may designate to Seller by notice in accordance with Paragraph 10(b) and, if no such address has been designated, to the address of Buyer as set forth in Paragraph 21. Seller shall be the importer of record on all shipments into the United States. Buyer's part numbers, quantities and symbols shall be marked on all invoices, packages, bills of lading, shipping orders and correspondence, provided Seller shall have been timely notified thereof. Shipping memoranda or packing lists shall accompany each shipment of the Products, and, in the event that more than one package is shipped at one time, Seller shall identify the package containing the memoranda or lists. Two (2) copies of packing slips or shipping receipts shall be sent to Buyer on date of shipment.

(b) Seller shall select the least expensive mode of transportation and carrier consistent with the delivery requirements of Buyer, unless otherwise instructed by Buyer. The carrier shall be deemed to be Buyer's agent, except in the case of shipments from Seller's manufacturing facilities outside the United States to ports of entry in the United States selected by Seller for subsequent shipment to Buyer or its agent in the United States, in which case Seller shall be importer of record as aforesaid and the carrier shall be deemed Seller's agent, provided, however, that notwithstanding the foregoing, Buyer shall remain responsible for the payment of all charges pursuant to Paragraph 7.

7. Payment Terms.

(a) Prices set forth in Exhibit A are effective at Seller's shipping plant and do not include any freight, transportation, duties, insurance, sales, property or ad valorem taxes, all of which shall be at Buyer's expense.

(b) If Seller ships the Products in installments, each installment shall be deemed to be a separate delivery for the purpose of this paragraph. Seller will invoice all Products sold hereunder as either Game Sets and Cartridge Sets except in the event of purchase orders for individual spare parts, repair or replacement parts, or at Buyer's specific request. For delivery in the United States or other designated areas where the Products must clear customs, the terms of payment shall be thirty (30) days after the date of invoice, said date of invoice shall be approximately the date on which Seller shall deliver the Products to the appropriate port of entry. For delivery of products to locations without special customs requirements, such as Hong Kong, shipments shall be made F.O.B. Seller's plant to the Buyer's designated subcontractors and invoice date shall be date of delivery by Seller to carrier. The terms of payment in these instances shall be thirty (30) days after the date of invoice.

(c) In the event that Buyer rejects Products in accordance with any of the provisions of Paragraph 8, Buyer may, upon written notice to Seller, set off against outstanding amounts due to Seller, an amount equal to the price of the Products multiplied by the number of defective or incomplete Game Sets and/or Cartridge Sets which Buyer or Buyer's agent is holding pending receipt from the Seller of the items of the Products necessary to

make those Game Sets and/or Cartridge Sets complete and acceptable.

8. Inspection, Testing, Acceptance and Rejection.

(a) The Products purchased hereunder shall be subject to inspection, test and acceptance by Buyer in accordance with the standards and procedures set forth in Exhibit B, in the following manner:

(i) Buyer may inspect the Products at any reasonable place and time, including Seller's or Buyer's plant or any other point of destination designated pursuant to this Agreement. In the event that Buyer elects to inspect the Products at the Seller's plant, Buyer's inspector shall in no way interfere with, delay or otherwise obstruct the operation of Seller's factory and shall restrict his activities solely to the inspection of Products tendered by Seller. Acceptance of the Products by such inspector shall be in writing.

(ii) If Buyer shall, pursuant to Paragraph 11, designate an agent to perform such inspection and acceptance, the Products shall be deemed to be accepted by Buyer upon acceptance by such agent.

(b) At Seller's plant or within thirty (30) days of receipt of a shipment by Buyer or its agent, Buyer or its agent shall be entitled to reject any Products which, having been tested by Buyer in accordance with Exhibit B, do not meet the Specifications set forth therein. Buyer shall, at its option, either (i) individually test all parts, Game Sets or Cartridge Sets from a given lot in accordance with Exhibit B, or (ii) individually test a

random sample of the parts, Game Sets or Cartridge Sets in accordance with Exhibit B, such random sample to be selected in accordance with a one percent (1%) AQL on electrical specifications, a two and one-half percent (2-1/2%) AQL on package, lead dimensions and solderability in accordance with MIL-STD-105D Sampling Procedure, Inspection Level II, Single Sampling. For the purpose of this subparagraph, a "lot" shall mean the total number of Game Sets, Cartridge Sets or parts thereof covered by a single shipment memorandum. In the event Buyer or its agent shall, as a result of such test, determine that any Game Set, Cartridge Sets or parts (in the case of tests performed pursuant to clause (i) above) or any lot (in the case of tests performed pursuant to clause (ii) above) shall fail to meet the Specifications, Buyer or its agent may reject such Game Set, Cartridge Sets, parts, or lot (as the case may be).

(c) In the event Buyer elects to inspect the Products at other than Seller's plant, and Seller shall not receive written notification of non-conformity from either Buyer or its agent (as the case may be) within thirty (30) days of the receipt of a shipment of Products, said Products shall be deemed to be accepted.

(d) In the event Buyer or its agent shall reject any of the Products hereunder in accordance with subparagraph (b) above, Buyer shall promptly notify Seller thereof by telex or other similar means. Return of rejected lots and/or individual parts shall be accomplished in accordance with Exhibit E. Seller shall

be liable for all shipping charges to and from the location designated by it to the Buyer in connection with defective Products returned pursuant to this Paragraph 8.

(e) Any Products rejected in accordance with this Paragraph 8 and found to be non-conforming by Seller shall be repaired or replaced, at Seller's option. Seller shall repair or replace and ship such repaired or replaced Products in a timely manner giving due consideration to Buyer's production requirements. The term "timely manner" shall mean the next available shipment allowing due time for the processing of Seller's internal paperwork but no later than thirty (30) days after receipt of notice that any such Products have been rejected. Seller may perform any minor repair work at the inspection location of Buyer or its agent, provided such work does not interfere with Buyer's production activities. In no event shall Seller be liable to Buyer for Products that do not conform to the Specifications except for repair or replacement thereof as provided herein.

(f) Any Products shipped by Seller in the good faith belief that such Products are conforming and which are rejected in accordance with this Paragraph 8 or returned in accordance with Paragraph 9 and which are repaired or replaced in a timely manner (as defined in subparagraph (e) above) shall not be subject to rights of cancellation of the Buyer set forth in subparagraph (g) of this Paragraph 8, Paragraphs 9, 10 or 14 and Buyer shall accept delivery of all such repaired or replacement Products.

(g) Buyer shall have the right, upon written notice to Seller, to cancel that portion of a purchase order for any Products

rejected in accordance with this Paragraph 8 or returned to Seller in accordance with Paragraph 9 if such repaired or replacement Products are not shipped to Buyer within thirty (30) days after Seller's receipt of notice that any such Products have been rejected. Upon exercise of such right, Buyer will promptly return to Seller an equivalent number of Game Sets or Cartridge Sets absent the rejected or returned Products. Accordingly, the minimum and cumulative amounts set forth in Exhibit C shall be reduced by the number of Products (i.e., Game Sets and Cartridge Sets) so cancelled and returned to Seller. The Seller will prepare and forward to Buyer a revised Exhibit C within ten (10) days after receipt of all the cancelled Game Sets and Cartridge Sets, which revised Exhibit C will supersede the prior Exhibit C and will be binding on the parties in accordance with Paragraph 27.

(h) The parties shall meet from time to time, upon the reasonable request of either, to review possible approaches to reducing costs and prices, improving the Products, or otherwise advancing their mutual interests as set forth herein, but nothing therein shall be deemed to require either party to agree with any amendments or modification of the provisions of this Agreement.

9. Seller's Warranty.

(a) Seller represents and warrants to Buyer that the Products sold hereunder shall at the time of acceptance by Buyer and for a period of seven (7) months after the date code indicated thereon, conform to the Specifications. Seller will ship Products within four (4) weeks of their indicated date code.

Failure by Seller to ship within said four (4) week period will entitle Buyer to reject the subject individual parts, Game Sets or Cartridge Sets but not entire lots of the Products (subject to the terms of Paragraph 8(e), (f) and (g)) or to accept such quantity and extend the aforesaid seven (7) month warranty by the period of such shipment delay. Seller's liability under this warranty shall not extend to any other person or entity other than Buyer or Buyer's agent or Buyer's licensees and shall be limited to the repair or replacement, at Seller's option, of any defective Products. Seller shall use all reasonable efforts to repair or replace and ship Products returned pursuant to this subparagraph (a) in a "timely manner" as such term is defined in Paragraph 8(e). Buyer shall have the right to cancel rejected Products in accordance with Paragraph 8(g). Seller shall be liable for all shipping charges to and from the location designated by it to the Buyer in connection with defective Products returned pursuant to this Paragraph 9.

(b) Repaired Products, or Products delivered as replacements, pursuant to the provisions of Paragraphs 8(e) or 9(a) hereof, shall also be covered by the foregoing warranty in accordance with its terms, and the warranty period with respect to such repaired or replacement Products shall begin upon the date of shipment thereof as determined by the new date code indicated thereon or as otherwise provided in subparagraph (a) above.

(c) Seller shall have no liability under this warranty for:

(i) any costs and expenses incurred to remove the Products from any circuit board;

(ii) any Products which have been altered, replaced or repaired, or have been serviced by persons other than Buyer or its agents without Seller's consent, which consent shall not be unreasonably withheld;

(iii) defects or failures which are the result of mishandling, vandalism, negligence, abuse or misuse of the Products.

(d) The soldering of parts to a printed circuit board under generally accepted commercial practice shall not void this warranty, provided that such parts shall be removed from said boards in a manner which shall permit Seller to test such parts.

(e) THE FOREGOING EXPRESS WARRANTIES OF SELLER ARE EXCLUSIVE AND ARE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED. SELLER SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

10. Shipments.

(a) To facilitate Buyer's internal production planning, Seller shall supply Buyer with a weekly ten-week shipment forecast based on estimated shipments versus the production quantities ordered on Buyer's purchase orders and acknowledged by Seller which shall reflect a linear progression of shipments to Buyer throughout the term of this Agreement, insofar as may be practicable. Said shipment forecast is supplied for informational purposes only by the Seller and shall not supersede Seller's acknowledged shipment schedule. In addition, Seller shall, upon written request, provide Buyer with work-in-process data on a per part number basis, at all facilities where the Products are being manufactured. This data shall include work-in-process quantities in

wafer starts and fab, and throughput yield in wafer process, probe, assembly and finished goods. All data shall be yielded to give equivalent finished goods quantities per part. Seller shall provide Buyer on a weekly basis with an explanation concerning the failure to deliver the Products in accordance with the Seller's acknowledged shipment schedule, and a corrective action plan delineating specific action to be taken, e.g., a wafer loading recovery plan that will recover the quantities in arrears and/or any imbalance in Cartridge ROM patterns.

(b) Buyer will provide written shipping destination instructions on the Monday that falls before the first shipping date of the following month, covering that month's shipments. Buyer reserves the right to change said shipping destination instructions at any time up to seven (7) days prior to any scheduled shipment date if Seller fails to ship or advises Buyer that it will be unable to ship the quantity and/or Cartridge ROM pattern type as previously advised by Seller.

(c) Seller shall ship Products in complete matched tested Game Sets only, as defined in Exhibit A, unless otherwise directed by Buyer. Production requirements for multiple part cartridges shall be shipped in balanced ROM parts only (Cartridge Sets) unless otherwise directed by Buyer.

(d) Seller shall ship during any fiscal monthly period of Seller, Game Sets and Cartridge Sets in accordance with the quantities ordered on Buyer's purchase orders acknowledged by Seller, which shall be placed in accordance with Paragraph 5. In addition to any other rights of Buyer under this Agreement, Buyer may

defer payment of the portion of the invoices due and payable under the terms of this Agreement for a specific Cartridge ROM pattern that exceeds the quantities ordered by Buyer and acknowledged by Seller in excess of five percent (5%) unless such excess is requested by Buyer and acknowledged by Seller. Within five (5) days after the cumulative amount of such Cartridge ROM pattern shipped equals the cumulative amount ordered, Buyer shall submit to Seller all such deferred payments. Seller reserves the right to ship up to five percent (5%) overage of any specific Cartridge ROM pattern scheduled in a given month, however, this shall not be cumulative on any such Cartridge ROM pattern on a month to month basis, nor shall it be cumulative in total for all Cartridge Sets ordered. Seller will ship all Cartridge Sets against purchase orders in chronological order for each Cartridge ROM pattern purchased prior to shipping the same Cartridge ROM pattern against a subsequent open purchase order.

(e) The purchase of probed ROM wafers or tested die by Buyer shall be credited against Seller's obligation to satisfy the quantity requirements set forth in Exhibit C for Cartridge Sets on a good die per ROM wafer basis.

(f) In the event that Seller shall be more than thirty (30) days in arrears in shipping scheduled quantities of the Products (whether Game Sets or Cartridge Sets) in accordance with the schedule and terms and conditions set forth herein, which delay shall be caused by any reason, including, but not limited to, a failure of the Products to meet the Specifications, but specifically excluding any delay caused by an event described or intended by Paragraph 14 hereof, the Buyer may, at any time prior

to the time Seller ships the quantity so in arrears, upon notice to Seller, cancel without cost the purchase order relative to the quantity so in arrears, or any portion thereof. Accordingly, the minimum and cumulative amounts set forth in Exhibit C shall be reduced by the quantity of Products so cancelled. The Seller will prepare and forward to Buyer a revised Exhibit C within ten (10) days after receipt of Buyer's cancellation notice, which revised Exhibit C will supersede the prior Exhibit C and will be binding on the parties in accordance with Paragraph 27.

(g) All shipments of the Products by Seller which have not been cancelled in accordance with the terms of this Agreement shall be deemed due shipments under the terms and conditions herein, and this Agreement shall remain in full force and effect for the period required by Seller to complete shipment of the quantities of Products in arrears, unless such Products are subsequently cancelled by Buyer as provided herein. The Buyer's remedies set forth in Paragraphs 8, 9, 10, 14 and 15 for lateness of shipments or failure to ship in accordance with the acknowledged shipment schedule shall be the Buyer's sole and exclusive remedies.

(h) Seller shall employ the available capacity at the Seller's plants for the manufacture of the Products in the following order of priority:

Chandler, Arizona - Wafer C

Chandler, Arizona - Wafer B

Glenrothes, Scotland - Wafer B

Seller will use all reasonable efforts to minimize the use of its

Glenrothes facility recognizing the increased expense to Buyer in customs duties attributable to Products manufactured there.

(i) Seller will provide, at Buyer's request, all documentation necessary for Buyer to obtain Tariff Schedule of the United States (TSUS) 807 or 800 qualification for customs purposes. In addition, Seller will, at Buyer's request, assist Buyer in obtaining TSUS 807 qualification for Cartridge Sets and any other Game Set parts not currently qualified for TSUS 807.

11. Agency.

Buyer may at any time and from time to time, by notice to Seller, appoint agents for the performance of its duties related to the Products, including, but not limited to, inspections and acceptance, order release for shipment, receipt of shipments, settlement of claims, changes in the Products and Specifications and the like. Seller may rely on the advice and instructions of any such agent within the scope of such agent's authority as the same may be designated by Buyer in such notice. Buyer shall indemnify and hold Seller harmless from liability of any kind on account of any and all acts of any agent appointed by Buyer, provided such acts are within the scope of the agency.

12. Second Source.

(a) In the event that Seller shall not be able to perform this Agreement for the reasons set forth in Paragraph 14 hereof, or is otherwise unable to meet the acknowledged shipment schedule, Buyer may request in writing that Seller establish a second source of supply for those items of the Products which are delinquent against the acknowledged shipment schedule by a quantity

equal to the scheduled thirty (30) day supply. In such event, Seller shall use reasonable efforts to enter into an agreement with a subcontractor approved by Buyer (which approval shall not unreasonably be withheld) to manufacture the items and quantities of the Products specified by Seller for which Seller is so delinquent. Alternatively, with the approval of the Buyer, Seller may enter into an agreement with a subcontractor to produce appropriate quantities of other items of the Products which are not delinquent but which said subcontractor manufacture will permit the Seller to reallocate its resources to increase the production of those items of the Products which are delinquent. Seller shall provide Buyer with a performance plan including but not limited to milestones for quality approval of the subcontractor's Products and production schedules. Any such subcontractor shall be under the direction and control of the Seller and shall not sell Products directly to the Buyer.

(b) Should the Seller be unable to establish a subcontractor in accordance with Paragraph 12(a) hereof within sixty (60) days of the Buyer's written request, then the Buyer shall have the option of establishing a second source for those items of the Products, and specifically those mask numbers, for which the Seller is delinquent against the acknowledged shipment schedule by a quantity equal to the scheduled thirty (30) day supply, upon payment to the Seller of a lump sum of $10,000 for each mask number per second source, but without royalty payment as provided in Exhibit F until such time as said delinquency shall be eliminated. For the lump sum payment, Seller shall deliver to the Buyer or to

the second source the information identified in Exhibit F(3). All such Confidential Information provided by Seller hereunder shall be complete in all respects and conform to Seller's then current manufacturing practices. Seller shall also provide to each second source a maximum of ten (10) working man-days of engineering service for each mask number to assist each such second source in the manufacturing of the respective part. Such initial engineering services will be provided without additional charge to any second source; provided, however, Buyer will be liable for all transportation and living expenses of the Seller's engineers without the continental United States. Further, any additional engineering services in excess of the ten (10) working man-days required by any such second source shall be billed at a rate of $75 per hour plus transportation and living expenses. Seller's engineers shall be under the direction and control of the Buyer's engineering department while rendering such engineering services. Buyer agrees to pay or shall cause each such second source to pay Seller the royalty as shown in Exhibit F beginning with the time that said delinquency is eliminated. Said royalty payments shall be based on the selling price of such Products between the second source and Buyer. For the purposes of the cumulative quantity steps in royalty percentages, the sales of each such second source to the Buyer shall be counted cumulatively from the beginning of shipments by each such second source of a particular mask number part, including the delinquency quantity.

(c) Buyer may, at any time during the term of this Agreement or upon termination of this Agreement as provided in Paragraph

15, for the purpose of establishing a manufacturing source for any one or more of Products, acquire from Seller the Confidential Information set forth in Exhibit F(3), which Confidential Information Seller will promptly transfer and deliver to Buyer upon the payment to Seller of the lump sum amount of $10,000 per Product part for each proposed manufacturing source and an agreement to pay or cause each such manufacturing source to pay Seller a royalty as shown in Exhibit F. Said royalty payments shall be based on the selling price of such Product between the manufacturing source and Buyer shall be cumulative for each manufacturing source by Product part and not for the manufacturing sources or Product parts as a group. All such Confidential Information provided by Seller hereunder shall be complete in all respects and conform to Seller's then current manufacturing practices. As further consideration for the above payments, Seller shall also provide to each manufacturing source for each Product part a maximum of ten (10) working man-days of engineering service to assist Buyer or each such manufacturing source in the manufacture of each such Product. Such initial engineering services will be provided without additional charge to any manufacturing source; provided, however, Buyer will be liable for all transportation and living expenses of the Seller's engineers without the continental United States. Further, any additional engineering services in excess of the ten (10) working man-days required by any such manufacturing source shall be billed at a rate of $75 per hour plus transportation and living expenses. Seller's engineers shall be under the direction and control of the Buyer's engineering department while rendering such engineering services.

(d) (i) In association with or in addition to the provisions of Paragraph 12(c) and at its sole expense and liability, Buyer may at any time during the term of this Agreement or upon termination of this Agreement as provided in Paragraph 15, for the purpose of establishing a manufacturing source for any or all of the Products (or other parts equivalent in form, fit and function to the Products) acquire from Seller the Confidential Information set forth in Exhibit F(3) and (4), which Confidential Information Seller will promptly transfer and deliver to Buyer upon the payment to Seller of the lump sum amount of $20,000 per Product part per manufacturing source and an agreement to pay or cause such manufacturing source to pay to Seller a royalty as set forth in Exhibit F. Said royalty payments shall be based on the selling of such Product or its equivalent between the manufacturing source and Buyer and shall be cumulative for each manufacturing source per Product part or its equivalent and not for manufacturing sources or Products as a group. All such Confidential Information provided by Seller hereunder shall be complete in all respects and conform to Seller's then current manufacturing practices. As further consideration for the above payments, Seller shall provide to Buyer or each manufacturing source for each Product a maximum of ten (10) working man-days of engineering service to assist each such manufacturing source in the manufacture of each such

Product. Such initial engineering services will be provided without additional charge to any manufacturing source provided, however, Buyer will be liable for all transportation and living expenses of the Seller's engineers without the continental United States. Further, any additional engineering services in excess of the ten (10) working man-days required by any such manufacturing source shall be billed at a rate of $75 per hour plus transportation and living expenses. Seller's engineers shall be under the direction and control of the Buyer's engineering department while rendering such engineering services.

(ii) Buyer hereby grants to Seller the right to manufacture for Buyer any or all parts developed by Buyer or its manufacturing source pursuant to this subparagraph. If Seller elects to manufacture any such parts, it shall so notify Buyer and Buyer shall provide to the Seller all of the relevant technical information as set forth in Exhibit F(3) and (4) and provide to Seller a maximum of ten (10) working man-days of engineering service for each Product part. All such technical information provided by Buyer hereunder shall be complete in all respects and conform to Buyer's then current manufacturing specifications. In consideration for which, Seller shall pay Buyer $20,000 per Product part per manufacturing source and the royalties set forth in Exhibit F based on the selling price of the part between Seller

and Buyer.

(e) In association with or in addition to the provisions of Paragraph 12(c) and at its sole expense and liability, Buyer may at any time during the term of this Agreement or upon termination of this Agreement as provided in Paragraph 15 establish a manufacturing source for any or all of the Products (or other parts whether or not equivalent in form, fit or function to the Products) independent of the Seller's tooling but utilizing less than a substantial portion of Seller's Confidential Information. In such event, Buyer and Seller shall negotiate in good faith to determine: (i) the amount of consideration, including both lump sum and royalties, Buyer shall pay Seller for the use of Seller's Confidential Information. Such royalty, if payable, will bear a direct relation to the ratio of Confidential Information used to the total technical information used in developing the Product measured against the royalty schedule set forth in Exhibit F; and (ii) the extent to which Seller shall provide further technical information and assistance to Buyer or the manufacturing source. Further, Buyer hereby grants to Seller the right to manufacture for Buyer any or all parts developed by Buyer or its manufacturing source pursuant to this subparagraph. If Seller elects to manufacture any such parts, it shall so notify Buyer and Buyer shall provide to the Seller all of the relevant technical information as set forth in Exhibit F(3) and (4) and provide to Seller a maximum of ten (10) working man-days of engineering service for each Product part. All such technical information provided by Buyer hereunder shall be complete in all respects and conform to

Buyer's then current manufacturing specifications. In consideration for which, Seller shall pay Buyer $20,000 per Product part per manufacturing source and the royalties set forth in Exhibit F based on the selling price of the part between Seller and Buyer.

(f) Any 40K cartridge ROM part manufactured for Buyer's Intellivision system which does not utilize Seller's Confidential Information, including by way of example, the ROM manufactured by American Microsystems, Inc. under mask set number Madiera 9397, shall be specifically excluded from the operation of Paragraphs 12(d) and (e).

(g) Seller represents that it has the right to sell and Buyer acknowledges that Seller may sell to third parties the Products (or other parts whether or not equivalent in form, fit and function) provided that Seller does not use or disclose Buyer's Confidential Information or violate any other of Buyer's property rights. Seller will handle all orders and deliveries for the Products, whether by Buyer or any third party, in accordance with Seller's standard order and delivery policies and practices. Specifically, Seller will not give preference or priority to orders or deliveries of any third party for the Products to the detriment of orders or deliveries of Buyer for the Products.

(h) Except for the provisions of Paragraph 21 with respect to patent indemnification and Paragraph 12(a), Seller shall not be responsible or liable to anyone, including Buyer, for the Products manufactured by any second source or manufacturing source under this Agreement.

(i) In the event a second source or manufacturing source is

established pursuant to subparagraphs (a) through (e) of this Paragraph 12, the Buyer or Seller will secure from each second source or manufacturing source a written obligation to protect the Confidential Information (as defined in Paragraph 16 hereof) of the parties and to observe and perform the necessary legal requirements to indicate and protect the trade secret, trademark, copyright and patent rights of the parties in and to the Products. If the requirements of the preceding sentence are adhered to, Buyer and Seller shall not make any claim or initiate any action alleging that such second source or manufacturing source has violated a trade secret, trademark, patent or copyright of the Buyer or Seller with respect to the Products.

13. Quality.

(a) In the event of recurring failures of the Products to meet the Specifications for the same or similar reasons or for non-correlation of test data, the quality control organizations of Buyer and Seller shall confer with respect to identification of the cause or causes of such failures and appropriate corrective action which might be taken.

(b) In addition to any test provided herein, Buyer may request Seller to provide data showing compliance with the tests in Exhibit D. In addition, Buyer may perform additional product qualification testing using Exhibit D as the basis for such testing. Buyer may communicate the results of such testing to Seller and, upon the written request of either party, the quality control organizations of Buyer and Seller shall meet to discuss such results and implement such action as they may deem appropriate.

Seller shall take corrective action within a reasonable time for any failure to perform or meet the standards of the tests provided in Exhibit D, but Buyer shall have no right of rejection for Products already produced.

(c) Seller shall perform periodic tests on the Products as defined in Exhibit G attached at its Chandler and Kaohsiung facilities. Seller shall maintain accurate records of such tests and shall report their results at periodic meetings with the Buyer. At Buyer's request, Seller will provide data on a weekly basis resulting from the tests performed. If any device in the Game Set fails to meet the 0.5% per item failure rate on a continual basis, Seller will, at no cost to Buyer, provide additional test/burn-in guardbands for such device.

(d) Seller and Buyer shall work cooperatively on a quality and reliabilty improvement program as documented in Exhibit H and as modified by mutual agreement from time to time. The Seller and Buyer shall meet periodically, but not less than once every sixty (60) days, to review the status of the actions described in Exhibit H.

14. Contingencies.

Seller shall not be liable for any delay in performance or for non-performance, in whole or in part, caused by the occurrence of any contingency beyond Seller's control, including, without limiting the generality of the foregoing, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of public enemy, failure or delay in transportation, act of any government,

agency or subdivision thereof directly affecting the terms of this Agreement, judicial decision or order, labor dispute, accident, fire, explosion, flood, storm or other act of God, or shortage of labor, fuel, supplies, materials or shortage of the Products due to catastrophic yield loss. Any such delays shall excuse Seller from timely performance, and Seller's time for performance shall be extended for a period after the cessation of the excused cause equal to the period of the delay, provided that Seller has made all reasonable efforts to cure such excused cause and to minimize such delay. If any such delay shall continue for a period of forty-five (45) consecutive calendar days, Buyer may, upon notice to Seller, cancel, without cost or penalty, the quantity or any portion thereof, of the Products which have not been shipped within forty-five (45) days of the acknowledged scheduled shipping date, provided such Products have not been shipped at the date of such cancellation notice. In the event of such cancellation, the minimum and cumulative amounts set forth in Exhibit C shall be reduced by the quantity so cancelled. The Seller will prepare and forward to Buyer a revised Exhibit C within ten (10) days after receipt of the Buyer's cancellation, which revised Exhibit C will supersede the prior Exhibit C and will be binding on the parties in accordance with Paragraph 27. Buyer's right of cancellation hereunder shall not be applicable to any quantities of the Products in arrears prior to the occurrence of any contingency, in which case Buyer's rights, if any, under Paragraph 10 shall apply. Further, Buyer's right of cancellation hereunder shall terminate thirty (30) days after the complete

cessation of each contingency that may occur. In the event of shortages of material, labor or capacity, Seller may allocate production and deliveries equitably among Seller's customers.

15. Termination.

(a) Seller may terminate its obligations hereunder to sell Products in accordance with Paragraph 5 and Buyer may terminate its obligation to purchase Products pursuant to Paragraph 5, in each instance, by the party desiring to terminate giving the other party at least thirty (30) days' prior written notice of such intent to terminate.

(b) In the event of a termination in accordance with Paragraph 15(a), Seller shall be obligated to manufacture and ship and Buyer shall be obligated to purchase and accept the acknowledged shipment schedule quantity of the Products at the effective date of termination including any quantities of Products in arrears on such date.

(c) In lieu of the obligation of Buyer as specified in the preceding paragraph, Buyer may elect in the termination notice to Seller, to pay termination charges equal to all costs (including direct labor, direct material and directly related manufacturing overhead costs, but excluding Seller's development costs) incurred and committed for all raw materials and goods in process at the date of the notice of termination. Buyer may, at its option and expense, request that all such termination charges be verified by Arthur Young & Company, provided, however, that any information disclosed by Seller to Arthur Young & Company shall

be deemed confidential and shall not be disclosed to Buyer.

(d) Termination pursuant to this Paragraph 15 shall not affect the rights or obligations of the parties under Paragraphs 9, 12, 16, 17, 19, 20, 21, 23, 24, 25 and 27 of this Agreement.

16. Confidential Information and Non-Disclosure.

The parties hereto acknowledge that certain of the information provided or to be provided in connection with the performance of this Agreement shall be deemed to be confidential, secret and/or proprietary (collectively "Confidential Information") by the disclosing party. Confidential Information shall mean any and all technical information and other information regarding the marketing plans and strategy, financial affairs, business, processes, apparatus, design and manufacture of products, researches, research programs and the like, now or hereafter in the possession of either party including, without limitation, documents, data or information relating to devices, processes, methods, materials, apparatus, design, research, yields and specifications. All Confidential Information shall be clearly marked "Confidential" and so communicated to the receiving party. Recipient acknowledges that the Confidential Information is a unique and valuable asset to the disclosing party. In consideration of the disclosure of any Confidential Information the parties agree as follows:

(a) Except as otherwise provided in Paragraph 12 hereof, the recipient shall not disclose at any time and shall use its best efforts to prevent its officers, employees or agents from disclosing at any time, appropriating or using on its own behalf or

on the behalf of others, any Confidential Information, without in each instance first obtaining the disclosing party's written consent thereto. The recipient shall restrict the circulation of Confidential Information to the same extent the recipient restricts its own proprietary information. Any Confidential Information which shall be circulated to employees of the recipient shall bear a legend to the effect that the information contained therein is proprietary to the disclosing party and that such information shall not be disclosed to other persons. The recipient further agrees to return to the disclosing party, upon written request, all such documents or other embodiments of any Confidential Information.

(b) The recipient shall not be obligated to maintain the confidentiality of any Confidential Information that the recipient can show:

(i) Is required to be disclosed by judicial decision or order after all reasonable legal remedies to maintain the confidentiality of such information have been exhausted; or

(ii) Is or becomes part of the public domain through no fault of recipient and only after it becomes part of the public domain. It being understood that any Confidential Information shall not be deemed to be in the public domain merely because it is embraced by more general information which may be in the public domain; or

(iii) Is known to the recipient or any of its subsidiaries prior to disclosure; or

(iv) Is approved in writing for public release by the disclosing party; or

(v) Is subsequently rightfully obtained by the recipient or any of its subsidiaries from a third party; or

(vi) Is independently developed by the recipient or any of its subsidiaries without any breach of this Agreement.

(c) The disclosing party, without limitation to any other remedies at law available to it, shall be entitled to appropriate equitable or injunctive relief in respect to any breach or anticipatory breach of this Paragraph 16 or Paragraph 12(g), without the necessity of proving damages.

(d) The provisions of this Paragraph 16 shall survive any termination or completion of this Agreement and shall remain in full force and effect for two (2) years after the date of such termination or completion except that all software codes developed by or for the Buyer in or for the Products shall be covered by said provisions indefinitely.

(e) All software ROM codes provided by Buyer are considered proprietary to Buyer and shall not be disclosed or sold to other parties without Buyers's prior written permission. These ROM codes include, but are not limited to, part numbers R0-3-9502-011, R0-3-9503-003, R0-3-9504-021 or their revised or replacement part numbers.

(f) Seller shall manufacture R0-3-9505-3XX 40K ROM, Mask Number 32046, exclusively for Buyer. Prior to the time Seller manufactures and ships goods utilizing said ROM Mask Number to third parties other than Buyer, Seller will refund to Buyer

$38,000.00 which Buyer paid to Seller as a partial development charge for said ROM Mask Number.

17. Publicity.

Seller shall submit to Buyer all advertising, sales promotion materials, press releases and other publicity matters relating to the Products furnished or the services performed by Seller under this Agreement, wherein the name of Buyer is mentioned or language from which the connection of said name therewith may be inferred or implied; and Seller shall not publish or use such advertising, sales promotion materials, press releases, or other publicity matters without Buyer's prior written approval. Buyer shall not make or issue any public statement, whether oral or written, with respect to Seller's prices, performance or quality hereunder without Seller's prior written approval.

18. Program Management.

Seller shall appoint and maintain throughout the Agreement term a program manager with complete responsibility for the production implementation of Buyer's program. This manager shall be a full-time resident at the Chandler facility with primary responsibility for those matters relating to the production schedule for the Products.

19. Limitation of Liability.

In no event shall either party be liable to one another or any third party for direct, indirect, incidental, special or consequential damages or expenses for: (a) breach of any of the provisions of this Agreement; and (b) the purchase and use of the Products. Without limiting the generality of the foregoing, such

excluded damages or expenses shall include costs of removal and installation of the Products, loss of goodwill, loss of profits or loss of use. All remedies provided in this Agreement shall be deemed to be the sole and exclusive remedies of the party having a right to invoke the same for the acts, defaults, breaches, events or causes for which such remedies are provided, except as otherwise expressly provided herein.

20. Patent Indemnity.

(a) Seller shall indemnify and hold Buyer and any second source or manufacturing source established pursuant to Paragraph 12 hereof harmless from any suit or proceeding brought against Buyer to the extent that such suit or proceeding is based on a claim that the process utilized by Seller to manufacture the Products or that the circuit layout of the Products constitutes a direct or contributory infringement of any valid United States trademark, copyright or patent.

(b) Buyer shall indemnify and hold Seller harmless from any suit or proceeding brought against Seller to the extent that such suit is based on a claim that the use of the Products or Buyer's end product constitutes a direct or contributory infringement of any valid United States trademark, copyright or patent.

(c) In the event of either (a) or (b) above, the indemnifying party shall pay all damages and costs awarded by final judgment (from which no further appeal may be taken) against the indemnified party, provided that the indemnifying party (i) is promptly informed and furnished a copy of each communication, notice or other action relating to the alleged infringement, (ii)

is given authority, information and assistance necessary to defend or settle such suit or proceeding in such manner as the indemnifying party shall determine, and (iii) is given sole control of the defense (including the right to select counsel), and the sole right to compromise and settle such suit or proceeding.

THE FOREGOING STATES THE SOLE AND EXCLUSIVE LIABILITY OF THE PARTIES HERETO FOR INFRINGEMENT OR THE LIKE OF PATENTS, TRADEMARKS AND COPYRIGHTS, WHETHER DIRECT OR CONTRIBUTORY, AND IS IN LIEU OF ALL WARRANTIES, EXPRESS, IMPLIED OR STATUTORY IN REGARD THERETO, INCLUDING, WITHOUT LIMITATION, THE WARRANTY AGAINST INFRINGEMENT SPECIFIED IN THE UNIFORM COMMERCIAL CODE.

21. Notices.

All notices or communications required, permitted or contemplated by this Agreement or desired to be given hereunder, shall be in writing addressed as follows and given by certified or registered mail, return receipt requested, or by telex and shall be deemed to be given when received:

If to Seller to:

General Instrument Corporation
Microelectronics Division
600 West John Street
Hicksville, New York 11802
Attention: Jo Ann Medigovich

and with respect to any notice of default or termination, with a copy to:

General Instrument Corporation
320 West 57th Street
New York, New York 10019
Attention: General Counsel

and, if to Buyer to:

Mattel, Inc.
Mattel Electronics Division
5150 Rosecrans Avenue
Hawthorne, California 90205
Attention: Anita Hollensed
Subcontracts Administrator

and, with respect to any notice of default or termination, with a copy to:

Mattel, Inc.
5150 Rosecrans Avenue
Hawthorne, California 90250
Attention: Law Department

22. Administration.

The administration of this Agreement shall be accomplished through Mattel Electronics, a division of Mattel Inc., having a place of business at 5150 Rosecrans Avenue, Hawthorne, California 90250, USA. All day to day administrative and other matters of a contractual nature will be coordinated and directed by a single representative of Buyer and Seller. Buyer hereby designates Karen Meyers as its representative. Seller hereby designates Jo Ann Medigovich as its representative. Such representatives may be changed at any time by notice pursuant to Paragraph 21. Any changes, communications or directives of an administrative nature given by either party which are not confirmed in writing by the above designated representatives shall not be binding upon either party.

23. Validity.

The invalidity in whole or in part of any term or condition of this Agreement shall not affect the validity of the rest of this Agreement or any other term or condition herein.

24. Waiver.

The failure by either party to enforce at any time or for any period of time any of the provisions of this Agreement shall not constitute a waiver of such provisions or of the right of such party to enforce each and every provision.

25. Governing Law.

The validity, construction and performance of this Agreement and the transactions to which it relates shall be governed by and construed under the laws of the State of New York.

26. Assignment.

This Agreement is binding upon and inures to the benefit of the parties hereto and the successors and assigns of the entire business and goodwill of either Seller and Buyer or that part of the business of either used in the performance of the Agreement, but shall not be otherwise assignable without the prior written consent of the other party. Notwithstanding the foregoing, Buyer may require Seller to ship the Products to Buyer's licensees or subsidiaries provided, however, that Buyer shall remain liable for the price of Products shipped to such licensees or subsidiaries. Nothing in this Paragraph or this Agreement shall inure to the benefit of or be deemed to give rise to any rights in any third party, whether by operation of law or otherwise, except as stated herein.

27. Merger.

This Agreement, including all Exhibits hereto, shall constitute the final, complete and exclusive written expression of all terms of the sale and purchase of the Products. Except as provided elsewhere herein, this writing shall supersede all previous communications, representations, agreements, promises or statements, either oral or written, with respect to the transactions contemplated herein and no such communications, representations, agreements, promises or statements of any kind made by either

party shall be binding on such party and each party hereby confirms that it is not relying upon any such communications, representations, agreements, promises or statements. No addition to or modifications of any provision of this Agreement or any Exhibit hereto shall be valid or binding unless made in writing and signed by the party to be charged.

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be signed by their respective duly authorized officers as of the day and year first above written.

MATTEL, INC.
Mattel Electronics Division

By_____
Joshua W. Denham
President - Mattel
Electronics Division

GENERAL INSTRUMENT CORP.
Microelectronics Division

By_____
E. A. Sack
Senior Vice President

EXHIBIT A

LIST OF PRODUCTS
GAME SET

Description	Parts for U.S. Version Game Set			Parts for PAL Version Game Set		
	Part #	CPS #	Rev.	Part #	CPS #	Rev.
CPU	CP1610	10036	F	CP-1610	10036	F
RAM	RA39600	10032	G	RA39600	10032	G
STIC	AY38900-1	10037	F	AY38900	10042	H
Exec. ROM-1	R039502-YYY	10031	F	R039502-YYY	10031	F
Exec. ROM-2	R039504-ZZZ	10040	F	R039504-ZZZ	10040	F
Graphics ROM	R039503-003	10030	F	R039503-003	10030	F
Color	AY38915-001	10035	F	Not Applicable		
Sound	AY38914	10034	G	AY38914	10034	G

Note 1: Executive ROMs shall have the following mask patterns:

	YYY	ZZZ
Standard Version	011	021
Sears Version	025	026

Other Executive ROM patterns may be defined from time to time in accord with the provisions of Paragraph 3 hereof.

Price of each Game Set shall be:

	G.I.
1st 525K	28.52
Next 525K	27.00
Next 525K	25.00
Thereafter	23.50

For purposes of spare part orders, repairs and replacements, the value of individual Game Set Parts shall be determined by using the following formula:

Game Part % of Game Set X Game Set Price= Game Part Price

Description	Part #	% of Game Set
CPU	CP1610	15.8
RAM	RA39600	20.3
STIC-US	AY38900-1	19.3
STIC-EUR	AY38900	22.8
Exec. ROM-1	R039502-YYY	12.3
Exec. ROM-2	R039504-ZZZ	9.6
Graphics ROM	R039503-003	9.6
Color	AY38915-001	3.5
Sound	AY38914	9.6

At such time as the Exec. ROM-1 and Exec. ROM-2 are replaced by a single Exec. ROM, the list of Products for a Game Set shall become:

Description	Parts for U.S. Version Game Set			Parts for PAL Version Game Set		
	Part #	CPS #	Rev.	Part #	CPS #	Rev.
STIC	AY38900-1	10037	F	AY38900	10042	H
CPU	CP-1610	10036	F	CP-1610	10036	F
RAM	RA39600	10032	G	RA39600	10032	G
Exec. ROM	R039506-AAA	10046	*	R039506-AAA	10046	
Graphics ROM	R039503-003	10030	F	R039503-003	10030	F
Color	AY38915-001	10035	F	Not Applicable		
Sound	AY38914	10034	G	AY38914	10034	G

*To be determined at a later date.

Note 2: Executive ROMs shall have the following mask patterns:

	AAA
Standard Version	TBD
Sears Version	TBD

Other Executive ROM patterns may be defined from time to time in accord with the provisions of Paragraph 3 hereof.

At that time, for purposes of spare parts orders, repairs and replacements, the value of individual Game Set Parts shall be determined by using the following formula:

Game Part % of Game Set X Game Set Price = Game Part Price

Description	Part #	% of Game Set
CPU	CP1610	16.7
RAM	RA39600	21.6
STIC-US	AY38900-1	20.6
STIC-EUR	AY38900	23.7
Exec. ROM	R039506-AAA	17.6
Graphics ROM	R039503-003	10.2
Color	AY38915-001	3.1
Sound	AY38914	10.2

EXHIBIT A (continued)

CARTRIDGE SET

Description	Parts for Cartridge Set Part # **	CPS #	Rev.
Cartridge ROM (20K)	R0-3-3-9504-1XX	10040	F
Cartridge ROM (20K)	R0-3-3-9504-2XX	10040	F
Cartridge ROM (40K)	R0-3-9505-3XX	10047	C

**"X" is a number from 0 to 9 assigned to identify specific Cartridge Part codes.

Prices of Cartridge Sets or Parts shall be as follows:

Quantity (in 20K Sets or 40K Parts)	Prices (Per 20K Set or 40K Part)
First 2.2 million	$3.00
Next 2.1 million	2.80
Next 2.1 million	2.50
Next 2.1 million	2.40
Thereafter	2.30

For purposes of individual cartridge part pricing, the value of each 20K Cartridge ROM shall be equal to 50% of the value of a Cartridge Set. Pricing for mixed Cartridge Sets (i.e., one 20K Part and one 40K Part) will be equal to 150% of the above applicable price.

Note 3: Game Parts to be shipped in matched sets unless otherwise requested in Buyer's purchase order. Specification for the U.S. Version of the Game Sets shall be CPS #10043.

Note 4: 20K ROM Cartridge parts to be shipped in sets unless otherwise requested by the Buyer.

Note 5: For the purposes of Exhibit C, a single ROM or a multiple of ROMs shall count as a Cartridge Set in accord with the ROM content of the cartridge.

Note 6: All Game Sets (e.g., U.S., PAL, SEARS, etc.) count equally for the purpose of calculating cumulative quantities toward the price steps.

Note 7: All Cartridge Set orders scheduled for shipment after August 1, 1982 will be completed with the shipment of one 40K ROM, except as otherwise requested by Buyer. All Cartridge Sets returned to Seller after August 1, 1982 for replacement pursuant to Paragraphs 8 and 9 will

be reshipped as one 40K ROM part provided Buyer returned a complete Cartridge Set (i.e., both 20K ROM parts) unless as otherwise requested by Buyer. If not, single 20K ROM replacement parts will be provided.

Note 8: All complete Game Sets returned to Seller for replacement pursuant to Paragraphs 8 and 9 of this Agreement will be credited to Buyer's account at the original invoice price. All repaired or replacement Game Sets therefor will be invoiced at a price of $22.50 (except for Game Sets returned pursuant to Paragraph 9(a) (i.e., date code beyond permissible four (4) week period) which Game Sets will be remarked and reinvoiced at original invoice price.).

EXHIBIT B

COMPONENT PROCUREMENT SPECIFICATIONS

OF THE PRODUCTS CONTAINED HEREIN

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
F	5/7/82	13103		REWRITTEN			

GI DRAWING
AND SPEC. CONTROL
VALID COPY

SHEET	1	2	3	4	5	6	7	8	9				
LAST REV	F	F	F	F	F	F	F	F	F				

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT — MICROELECTRONICS GROUP

TITLE: RO-3-9503 CUSTOMER PROCUREMENT SPEC.

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED					
BY	J.D.H.	[signature]	[signature]	[signature]	[signature]		[signature]
DATE	4/29/82	4/29	5/1/82	5/5/82	[signature]		4-29-82

SHEET 1 OF 9

SPEC. NO. CPS-10030

REV F

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the RO-3-9503 N-Channel MOS Graphics ROM (GROM).

2.0 CIRCUIT FEATURES

Mask programmable storage providing 2048 X 10 bit words.

16 Bit On-Chip Address Latch.

Memory Map Circuitry to place the 2K ROM page within a 65K memory area.

8 Bit Tri-State Bus with Higher 8 Bits Driver to Zero During Read Operations.

11 Bit, Static Address Outputs for external Memory.

Control Signals for External Memory.

$\overline{\text{ENABLE}}$

R/$\overline{\text{W}}$

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

4.1 FUNCTIONAL TESTING

The RO-3-9503 must be functional in the use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational as per Mattel specification) target failure rate for this device is 0.5 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0eV.

5.0 OPERATION DESCRIPTION

The device operates in three memory configurations. These configurations are selected via the input control signals.

1. When SR1 has been pulsed negative, the memory is located at 12288 to 14335. The external memory is addressed at 14336 to 16383.

2. When $\overline{\text{BUSAK}}$ has been pulsed negative, the memory is located at 0 to 2047. The external memory is addressed at 2048 to 4095.

3. When BAR' and DWS' are pulsed positive, the memory will not respond to address bit 9 and address bit 10, which restricts the memory to 512 locations. The memory is now located from Ø to 511 relative to the current memory origin. The external memory is also addressable from Ø to 511 relative to its current origin. Configuration three may be released by applying a negative pulse on the SR1 input.

FORM 15102 (4/82)

6.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vss	-0.2v to +9.0v
Vcc with respect to Vss	-0.2v to +9.0v

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Specification

Ambient Temperature	0°C to +55°C

DC CHARACTERISTICS

Vss = 0.0V, Vcc= +4.85V to +5.15V

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Bus/Control Inputs					
Input Logic Low	VIL	0	0.7	Volts	
Input Logic High	VIH	2.4	Vcc	Volts	
Input Leakage	IIL		5	uA	VIN = 0V to Vcc
Bus Outputs SB and YB					
Output Logic Low	VOL	0	0.5	Volts	IOL = 100uA, +100pf
Output Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA
Address Outputs					
Output Logic Low	VOL	0	0.5	Volts	IOL = 500uA, +100pf
Output Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA
Control Outputs					
Output Logic Low	VOL	0	0.5	Volts	IOL = 100uA, +100pf
Output Logic High	VOH	2.4	Vcc	Volts	IOH = 100ua
Supply Current					
Vcc	Icc		100	mA	at +55°C

A.C. CHARACTERISTICS

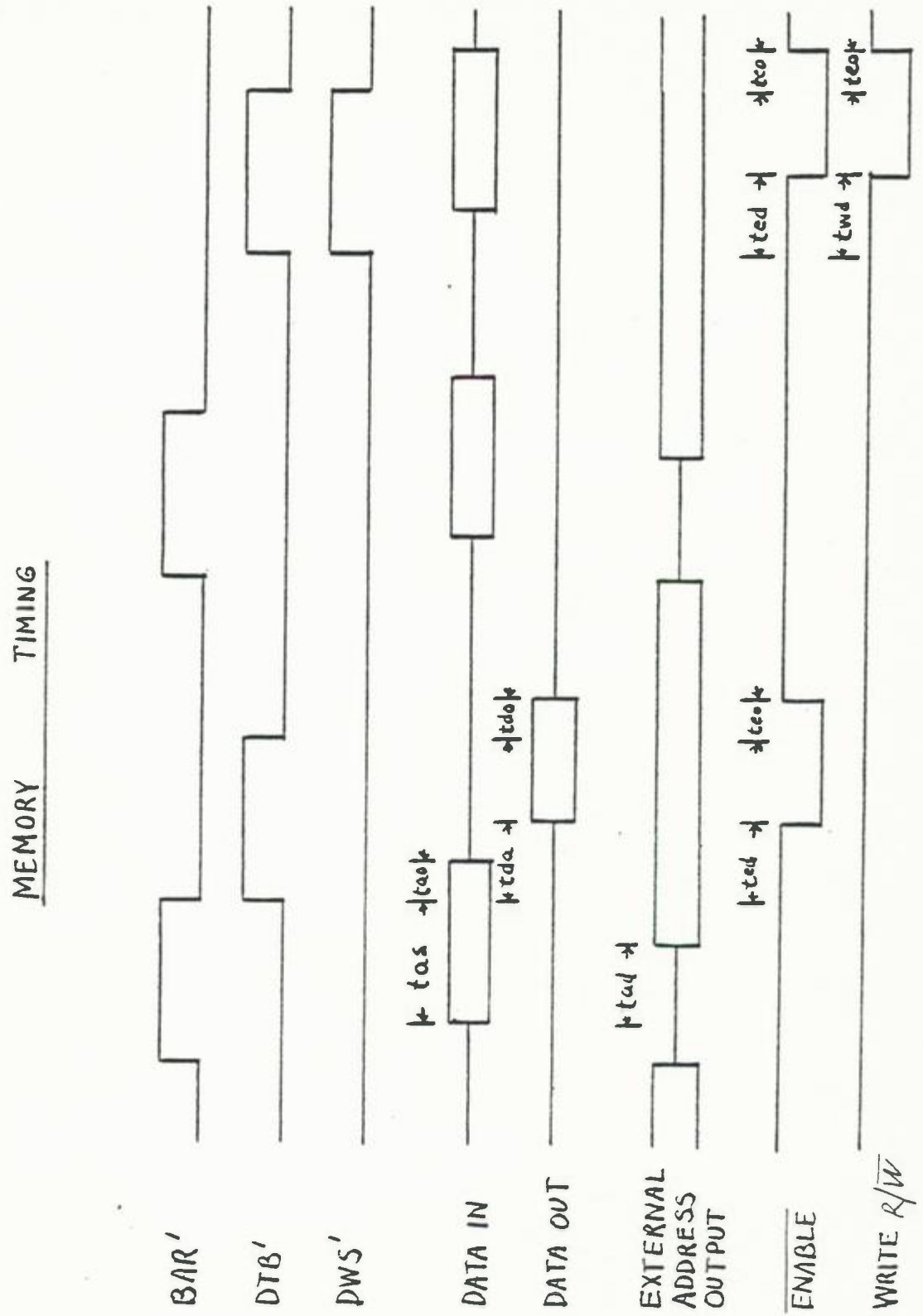
CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Bus Inputs SB and YB					
Address Set Up	tas	100		nSec	
Address Overlap	tao	50		nSec	
Bus Outputs SB and YB					
Turn On Delay	tda		550	nSec	
Turn Off Delay	tdo	0	250	nSec	
Address Outputs					
Turn On Delay	tad		300	nSec	from data bus valid
Control Outputs					
Enable and Write Turn On Delay	ted,twd		300	nSec	from DTB' and DWS'
Turn Off Delay	teo		200	nSec	

Note: Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz
Not measured during production test

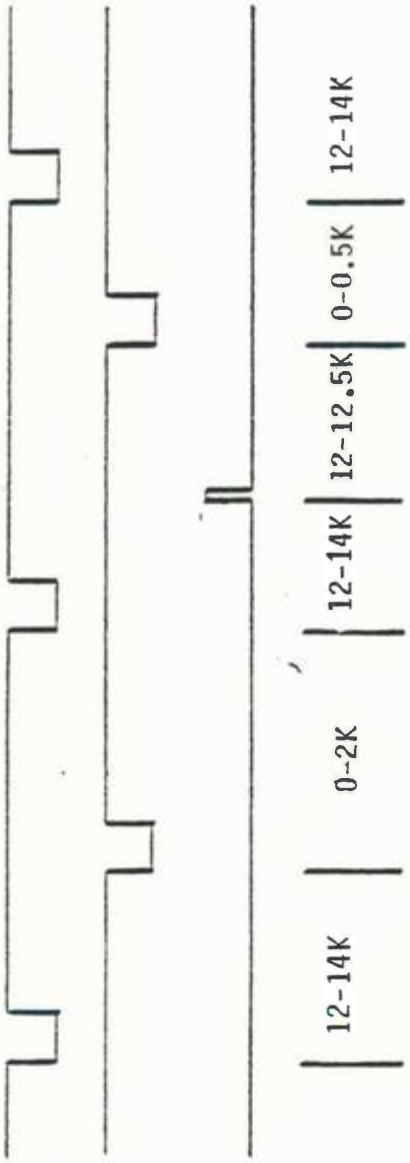
6.0 PIN CONNECTIONS

1	Vcc	40	R/$\overline{W}$
2	SR1	39	$\overline{ENABLE}$
3	$\overline{BUSAK}$	38	DWS'
4	SB15	37	DTB'
5	Not Connected	36	BAR'
6	SB14	35	Not Connected
7	SB13	34	Y_{BO}
8	SB12	33	ADDR 0
9	SB11	32	YB_1
10	No Connect	31	ADDR 1
11	SB10	30	Y_{B2}
12	No Connect	29	ADDR 2
13	SB9	28	YB3
14	ADDR 8	27	ADDR 3
15	SB8	26	Not Connected
16	$\overline{MSYNC}$	25	SB4
17	ADDR 7	24	ADDR 4
18	SB7	23	$_{S}B5$
19	ADDR 6	22	ADDR 5
20	SB5	21	Vss

MEMORY TIMING

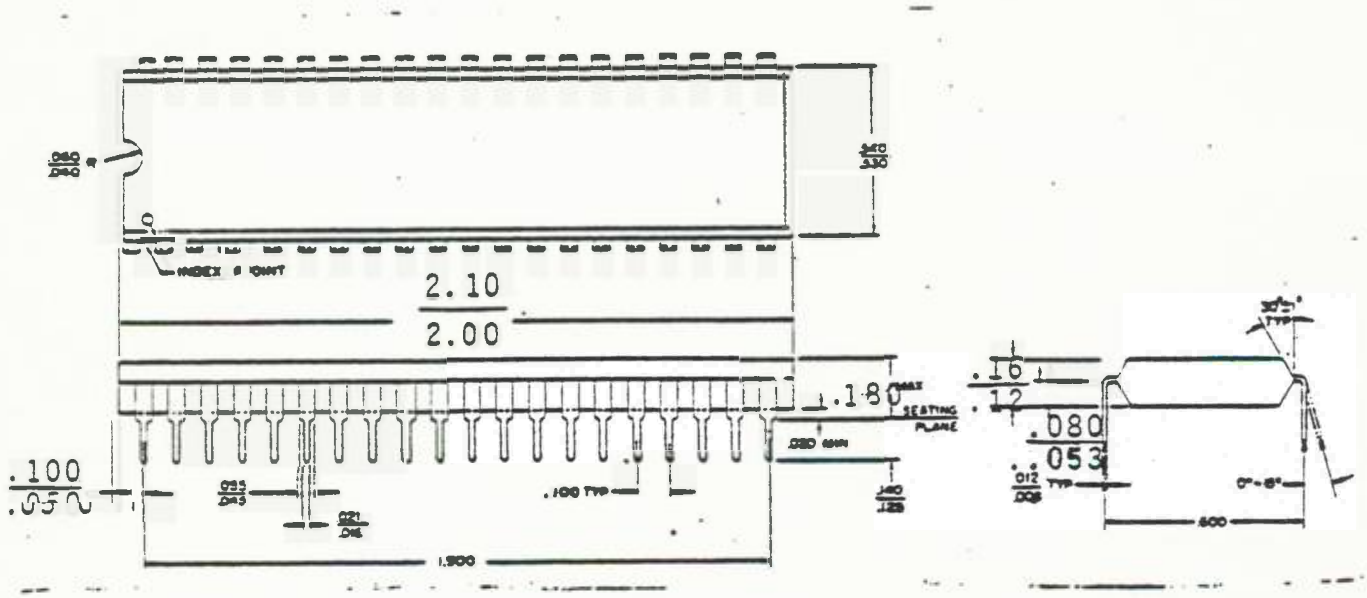


MEMORY POSITION RELATIVE TO CONTROL OPERATION



7.0 MECHANICAL CHARACTERISTICS

7.1 PACKAGE DIMENSIONS



7.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2 Aging.

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
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F	5/7/82	13103		REWRITTEN			

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AND SPEC. CONTROL
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SHEET													
LAST REV													

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GENERAL INSTRUMENT

MICROELECTRONICS GROUP

PLANT

MODULE

OPERATION

TITLE

RO-3-9502 CUSTOMER PROCUREMENT SPEC

	WRITTEN	APPROVED					SHEET 1 OF 9	
BY	G.D.M.C.	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	SPEC. NO.	REV
DATE	4/29/82	729	5/1/82	5/5/82	[illegible]	4/29/82	CPS-10031	F

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the RO-3-9502 N-Channel MOS ROM IC. The pattern programmed into this ROM defines the lower EXEC area and is designated 011.

2.0 CIRCUIT FEATURES

Mask programmable storage providing 2048 X 10 bit words.

16 bit on-chip address latch.

Control decoder.

Programmable memory map circuitry to place 2K ROM page within 65K word memory space located on 2K page boundaries.

Master Reset logic with programmable 16 bit vectored start address.

Interrupt logic with programmable 16 bit vectored interrupt address.

16 bit static address outputs for external memory.

Control signals for external memory

ENABLE= (DTB + DWS). Address External

WRITE = DWS. Address External

Programmable memory map selection for external memory area.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in the CPS.

4.1 FUNCTIONAL TESTING

The RO-3-9502 must be functional in the use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.5 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0ev.

5.0 CIRCUIT REQUIREMENTS

The RO-3-9502 operates as the program memory for systems using a CP1610 series microprocessor.

It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

6.0 OPERATING DESCRIPTION

The RO-3-9502 is initialized by the $\overline{\text{MSYNC}}$ input and from the positive edge of this signal, it remains in a tri-state output condition, awaiting the IAB response. During the IAB, the 9502 transmitts a 16 bit code onto the external bus thus providing the system start address vector. The completion of the MCLR sequence is recorded on chips such that any further IAB Codes output the second interrupt vector. For initialization, the 9502 waits for the first address code. For this address code and all subsequent address sequences, the 9502 reads the 16 bit external bus and latches the value into its address register. The contents of this address register are made available for connection to external memory and are supplied on 16 latched outputs.

The 9502 contains a programmable memory map location for its own 2K page and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9502 will output the 10 bits of addressed data and also drive a logic zero on the top six bits of the bus.

6.1 INPUT CONTROL SIGNALS

BDIR	BCI	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	IAB
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	-
1	1	0	DW	-
1	1	1	INTAK	BAR

OPERATION WITH EXTERNAL MEMORY

The 16 bits from the address register are provided as static outputs for connection to external ROM or RAM devices. Two other signals are provided to control the external memory area. An enable signal is provided for any read or write operation, and a write signal, for any move out operation. The two external memory control signals are gated by a min-max memory map comparator. The minimum and maximum values are programmable on boundaries within the 65K word memory area. The memory map comparator for external memory is a simple single compare and the operation is such that when a 2K area is chosen, a five bit compare is used and for a 4K area a four bit compare, etc. The effect of this is that 2K pages may start on 2K boundaries, i.e., 0, 2, 4, 6, 8, etc., but 4K pages must be on 4K boundaries, i.e., 0, 4, 8, 12, etc. The same is true for 8K and 16K pages.

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to VSS	-0.2v to +9.0v
Vcc with respect to Vss	-0.2v to +9.0v

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Specification

Ambient Temperature	0°C to +55°C

DC CHARACTERISTICS

Vcc= +4.85V to +5.15V, Vss = 0.0V

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Input Logic Low	VIL	0	0.7	volts	
Input Logic High	VIH	2.4	Vcc	volts	
Input Leakage	IIL	-	5	uA	VIN = 0V to Vcc
CPU Bus Outputs					
Output Logic Low	VOL	0	0.5	volts	IOL = 1.5ma] +150pf
Output Logic High	VOH	2.4	Vcc	volts	IOH = 80uA]
Address and Enable Outputs					
Output Logic Low	VOL	0	0.5	volts	IOL = 1.0ma] +100pf
Output Logic High	VOH	2.4	Vcc	volts	IOH = 100uA]
Supply Current					
Vcc Supply	Icc	-	90	ma	at +55°C

7.0 con't.

AC CHARACTERISTICS

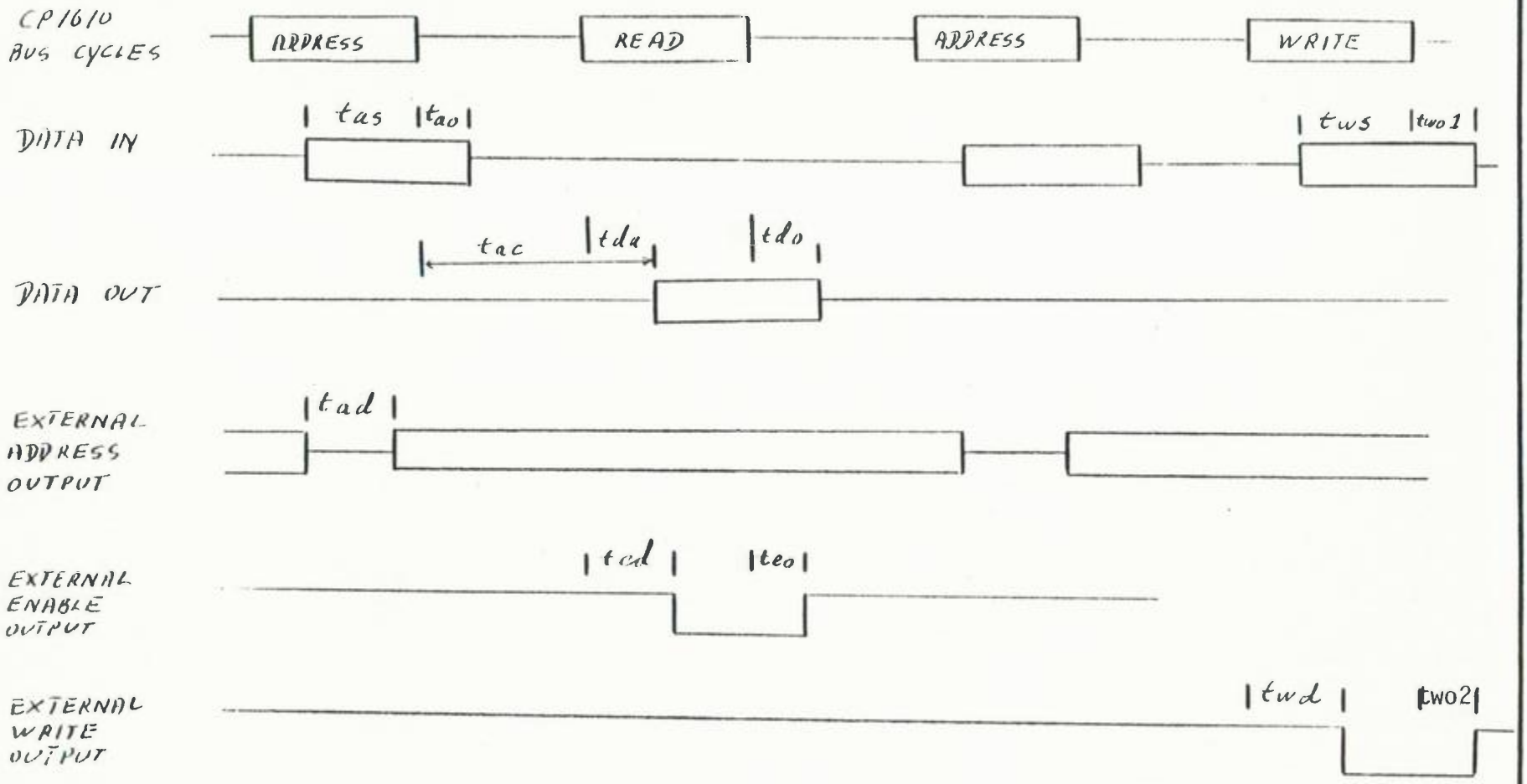
CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address Set Up	tas	300		nSec	
Address Overlap	tao		65	nSec	
Write Set Up	tws	300		nSec	
Write Overlap	two 1	200		nSec	
CPU Bus Outputs					
Turn ON Delay	tda	-	350	nSec	
Turn OFF Delay	tdo	80	250	nSec	
Access Time	tac		1.5	uSec	
Address and Enable Outputs					
Turn ON Delay	tad,tec	-	200	nSec	
Turn OFF Delay	teo	-	150	nSec	
Turn ON Delay	twd	-	300	nSec	
Turn OFF Delay	two 2	-	150	nSec	

Note: Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz. Not measured during production test.

8.0 PIN CONNECTIONS

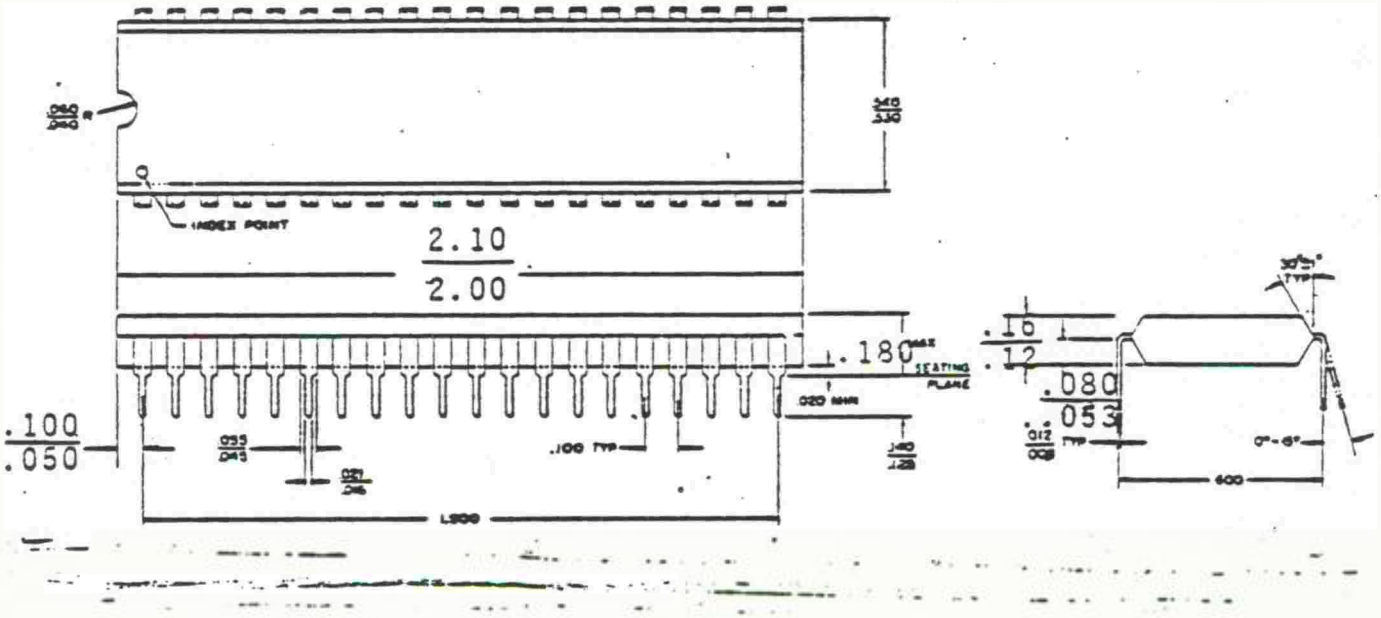
1	Vcc	40	BC 1
2	$\overline{RE}$	39	BC 2
3	R/$\overline{W}$	38	BDIR
4	No Connect	37	DB 0
5	DB 15	36	ADDR D
6	No Connect	35	DB 1
7	DB 14	34	ADDR 1
8	No Connect	33	DB 2
9	DB 13	32	ADDR 2
10	No Connect	31	DB 3
11	DB 12	3D	ADDR 3
12	No Connect	29	DB 4
13	DB 11	28	ADDR 4
14	No Connect	27	DB 5
15	DB 10	26	ADDR 5
16	ADDR 9	25	DB 6
17	DB 9	24	ADDR 6
18	ADDR B	23	DB 7
19	DB 8	22	ADDR 7
2D	$\overline{MSYNC}$	21	Vss

MEMORY TIMING



9.0 MECHANICAL CHARACTERISTICS

9.1 PACKAGE DIMENSIONS



9.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2 Aging.

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
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GENERAL INSTRUMENT

MICROELECTRONICS GROUP

PLANT

MODULE

OPERATION

TITLE

STIC SYSTEM RAM RA-3-9600/RA-3-9600-1
CUSTOMER PROCUREMENT SPECIFICATION

	WRITTEN	APPROVED					
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]
DATE	4/29/82	4/29	5/1/82	5/5/82	[illegible]		4/29/82

SHEET 1 OF 13

SPEC. NO. CPS-10032

REV G

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the RA-3-9600 N-Channel MOS data control RAM IC. This specification also contains the recommended system circuit for test acceptance.

2.0 CIRCUIT FEATURES

- o Memory area 352 words of 16 bits.
- o Address counter and control logic for D.M.A. operation.
- o Control decoder for CPU data control signals.
- o Memory map comparator and control logic for additional memory on 14 bit bus.
- o Current line buffer - 20 words of 14 bits.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

4.1 FUNCTIONAL TESTING

The RA-3-9600 must be functional in the use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.85 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0eV.

5.0 FUNCTIONAL DESCRIPTION

The RA-3-9600 is a 'dual port' interface and 16 bit wide RAM storage area. The RA-3-9600 contains twenty 14 bit serial data buffer registers with separate bus control signals.

The RA-3-9600 memory is 352 x 16 bit contiguous words from address 512-863 with the graphics descriptors using the first 240 words. The graphics use only the lower 14 bits of each word leaving the two most significant bits available for user storage.

6.0 OPERATION DESCRIPTION

The RA-3-9600 RAM accepts data from the CPU via a 16 bit bi-directional bus which is time multiplexed with address and data. A 3 bit control bus from the CPU is used to provide strobe signals for the on-chip address latch and main memory area.

The RAM has two operating modes:

Mode 1 - On decoding an interrupt the RAM is enabled into a bus copy mode.

In this mode the RAM copies the lower fourteen bits of the CPU bus onto the graphics bus. The direction of copy is always from the CPU and towards the graphics bus except during a bus reversal condition. The reversal condition is indicated when the CPU requests a read from an external graphics address on the 14 bit bus. Under this condition the 9600 will gate the 14 bit bus through to the 16 bit CPU bus.

Mode 2 - Is selected when the CPU issues the $\overline{\text{BUSAK}}$ signed (DMA acknowledge). The effect of $\overline{\text{BUSAK}}$ inside the 9600 is to reset the interrupt synchronizing logic and to switch the address decoder from the CPU address register to the graphics address counter. This counter, which sequences through the 240 words of graphics data, will have been previously set to zero when the interrupt signal was decoded. When the CPU is in the DMA state, the graphics system will prepare to display a new row of twenty characters and to load the 20 word buffer registers within the 9600. For the first cycle of DMA afer interrupt the graphics address counter will be at zero and the data at that address is passed to the 14 bit output. The action of SR3 will enable the output buffers and drive the 14 bit bus. The twenty shift registers are also loaded at this time. The negative edge of SR3 tri-states the 14 bit output and increments the graphics address counter. The shift registers are also clocked at this time. The SR3 input provides twenty positive pulses to the 9600 and loads the shift register buffers while giving the graphics bus the first row of characters. At the end of the first DMA cycle, after the CPU interrupt, the graphics address counter will be at value 19. The 9600 operation for the next fifteen lines will be to clock the 20 word shift registers and gate the contents onto the 14 bit bus under control of the SR3 input. When the CPU is running and $\overline{\text{BUSAK}}$ is a logic 1, the graphics address counter is not incremented. At the end of the first row of characters, the complete DMA operation is repeated. This sequence occurs for the 12 rows of characters until all 240 have been successfully accessed.

The operation of SR3, INCREMENT/TRI-STATE signal, is to step the shift register sequentially through each of the twenty characters. If the $\overline{BUSAK}$ signal is low, i.e., in DMA, it also increments the graphics address counter. SR3 disables the 14 bit graphics bus during the low period.

At the end of active picture the STIC issues an interrupt request to the CPU. The RA-3-9600 tests for the INTAK* response from the CPU and uses this signal as an entry control for a copy mode between the two buses. The end of the copy mode is controlled by the first $\overline{BUSAK}$ negative edge.

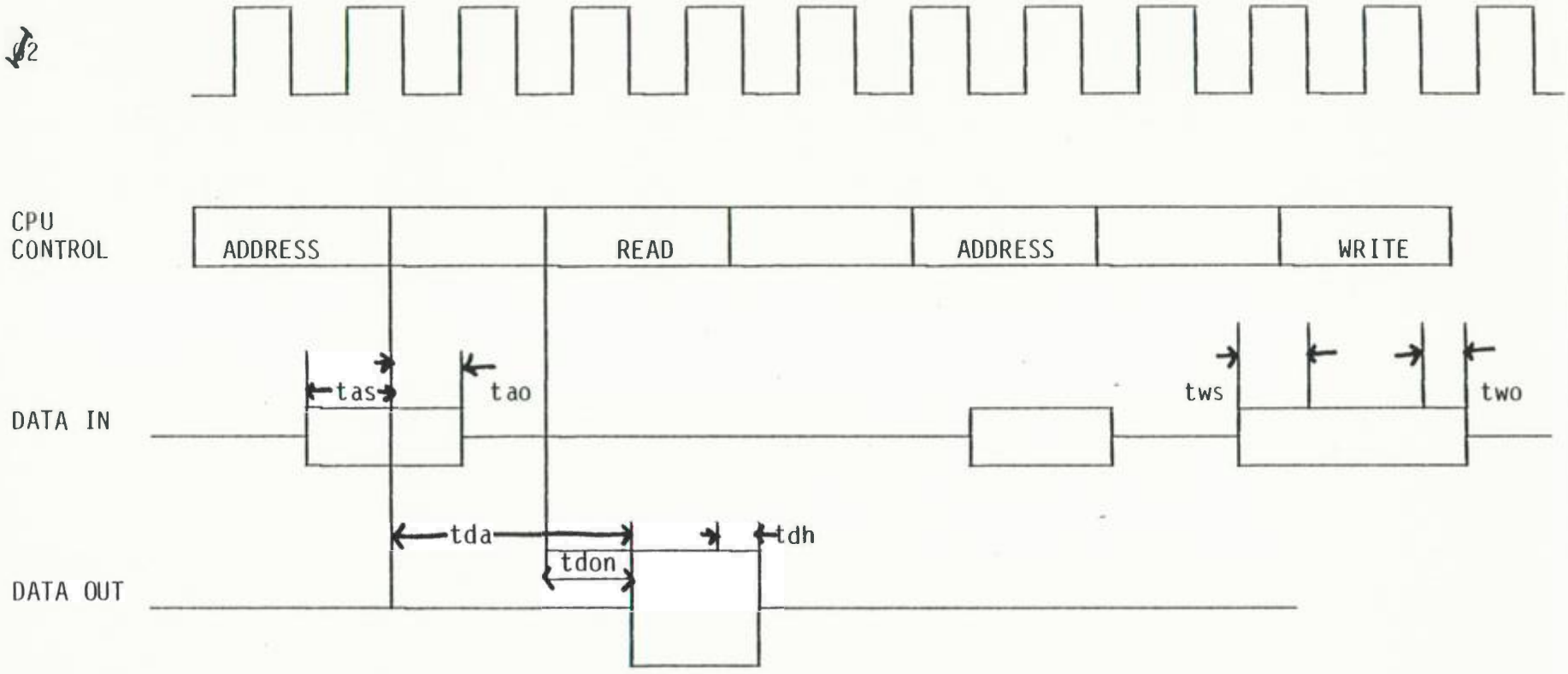
*INTAK, equivalent BC1, BC2, $B\overline{U}IR$ = '1'

A.C. CHARACTERISTICS

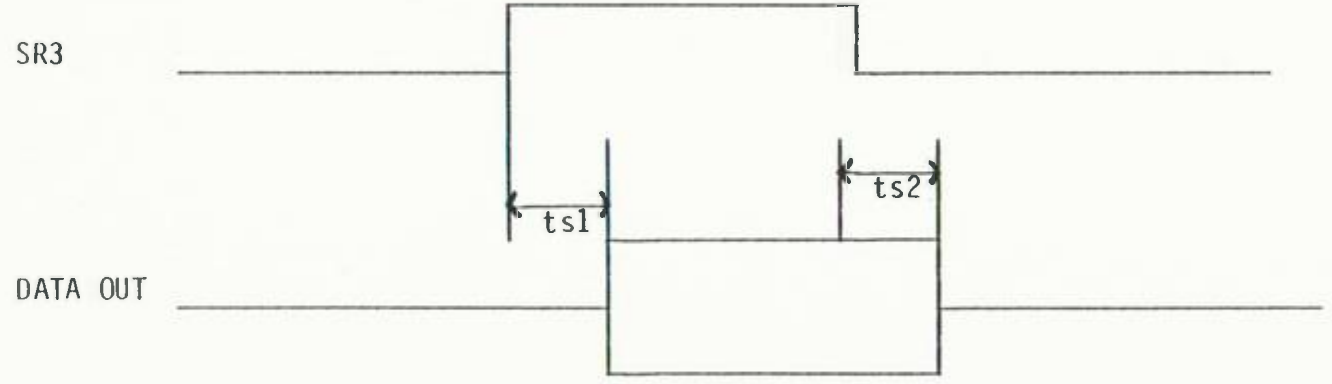
CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Input Ø2					
Period	tcy	0.5	0.560	uSec	Note 2.
Pulse Width	tØ2	160		nSec	either logic level
Rise and Fall Time	tr,tf		50	nSec	
CPU Bus Timing DB0-DB15					
Address Set Up Time	tas	300		nSec	
Address Hold Time	tao		50	nSec	
Data Access Time	tda		1.5	uSec	Figure 1
Data Turn-On Time	tdon		450	nSec	
Data Hold Time	tdh	0	250	nSec	
Write Set Up Ø2	tws	100		nSec	
Write Hold Ø2	two	200		nSec	
Bus Copy CPU -->STIC					
SR3 Valid and Date Changed	tcs		160	nSec	Figure 3
Bus Copy STIC -->CPU					
DTB and Data Changed	tsc		350	nSec	Figure 4
Shift Register Read					
SR3 Turn-On	ts1		250	nSec	Figure 1
SR3 Turn-Off	ts2	40		nSec	
*NTSC modifications:					
Data acces's time	tda		1.7	uSec	
Data Turn-On time	tdon		540	nSec	
Bus copy CPU -->STIC			220	nSec	

Note 2. RA-3-9600-1 (NTSC) 0.560uSec MIN

Note 3. Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz.
Not measured during production test.

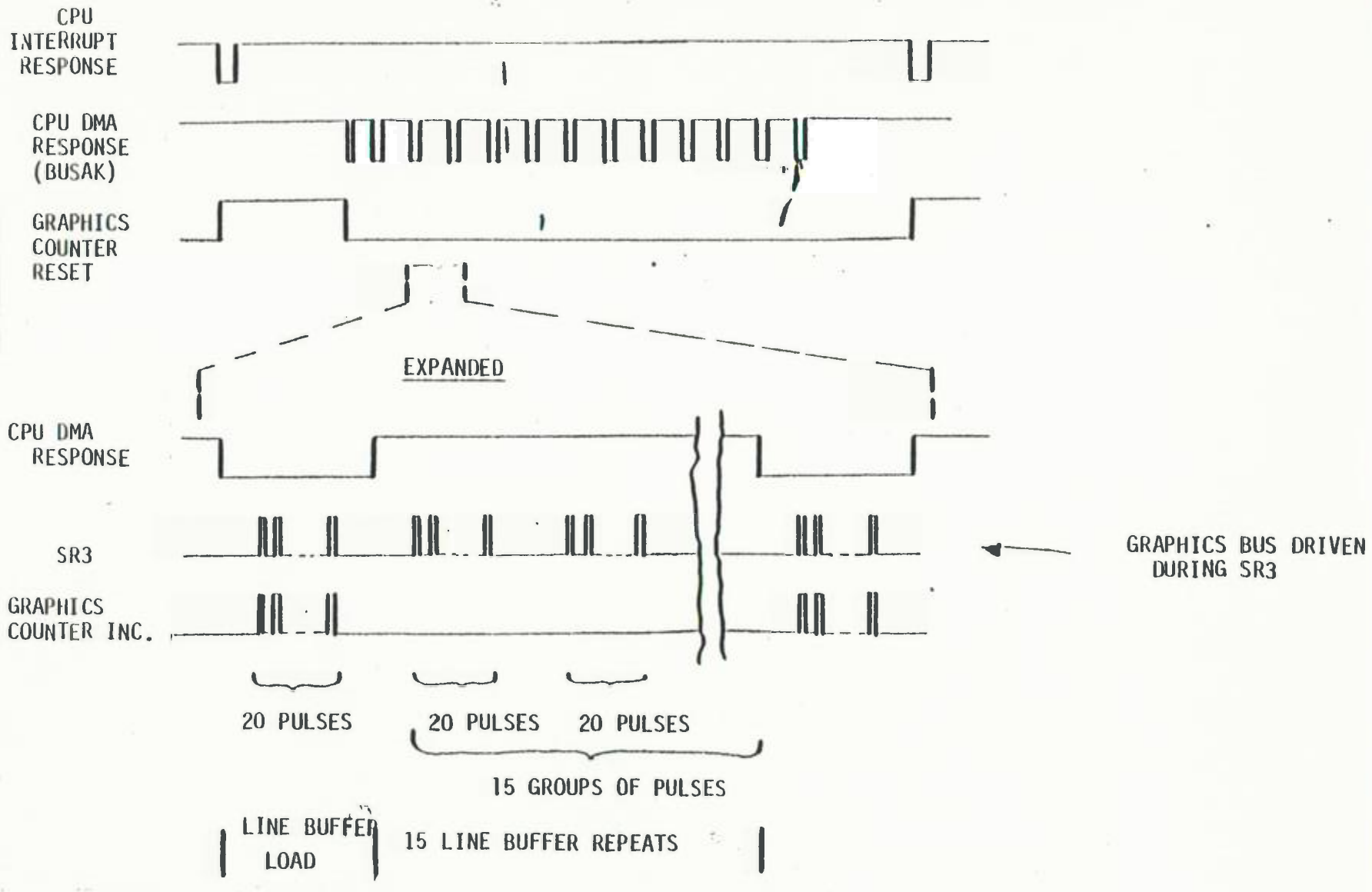


CPU BUS TIMING (16 BIT)



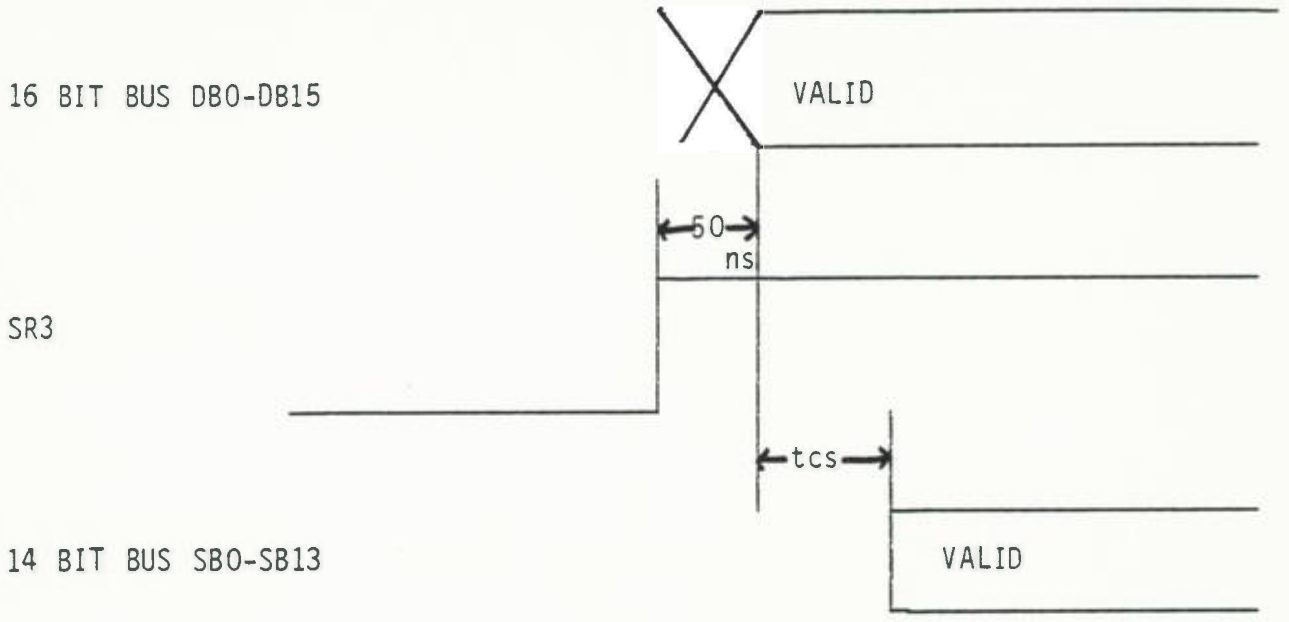
GRAPHICS BUS TIMING (14 BIT)

Figure 1



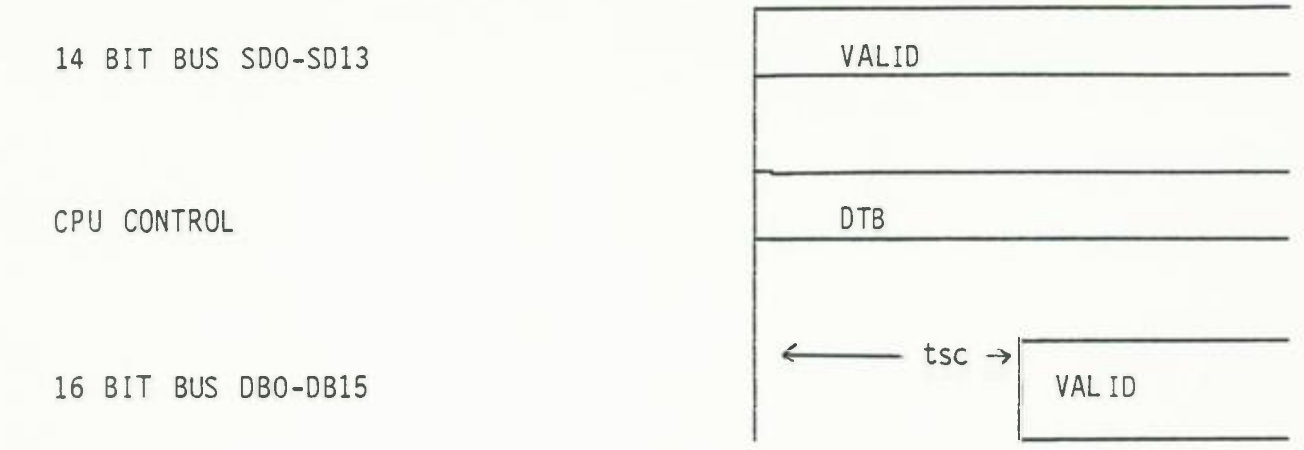
RAM GRAPHICS OPERATION

FIG. 2



CPU STIC BUS COPY

FIGURE 3



STIC - CPU BUS COPY

FIGURE 4

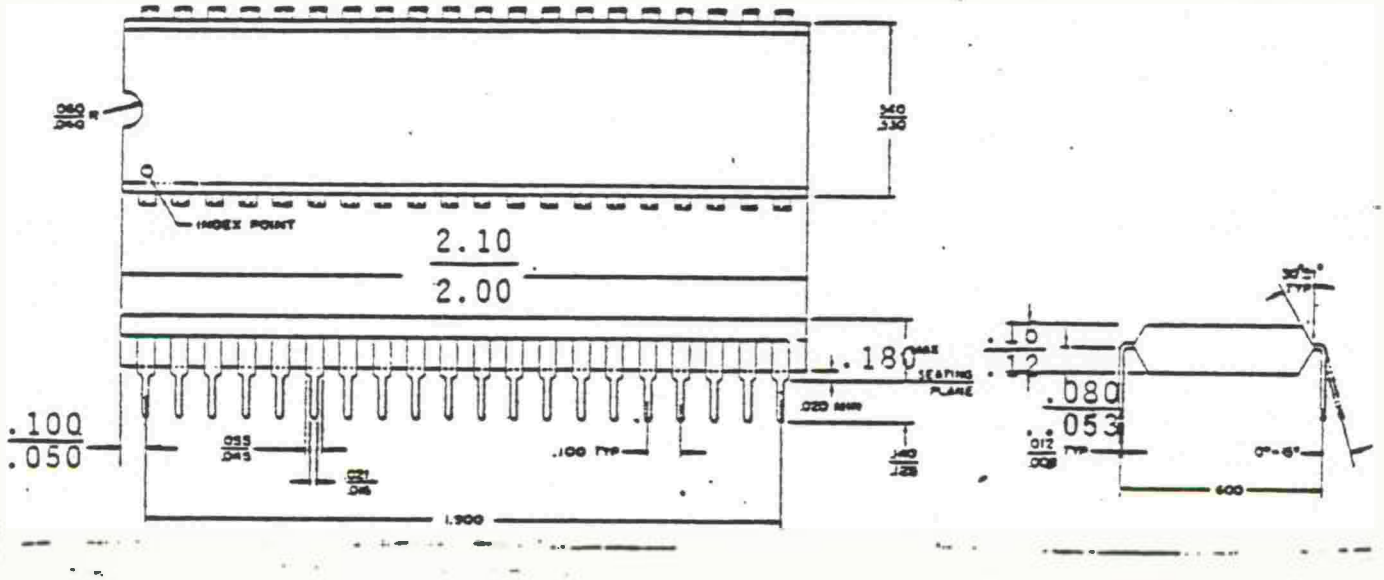
8.0 PIN CONNECTIONS

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	OB6	21	DB12
2	DB7	22	SB12
3	SB7	23	SB13
4	SB8	24	OB13
5	OB8	25	DB14
6	DB9	26	DB15
7	SB9	27	DBO
8	Ø2	28	SBO
9	Vcc	29	SB1
10	Vdd	30	DB1
11	Vbb	31	Vss
12	$\overline{\text{BUSAK}}$	32	SB2
13	SR3	33	DB2
14	BC 1	34	OB3
15	BC 2	35	SB3
16	BDIR	36	SB4
17	DB10	37	DB4
18	SB10	38	OB5
19	SB11	39	SB5
20	DB11	40	SB6

DB - Data Bus
SB - Graphics Bus

9.0 MECHANICAL CHARACTERISTICS

9.1 PACKAGE DIMENSIONS



9.2 SOLDERABILITY

The pins on the integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

9.3 MARKING

Devices which pass only American Timings are marked as RA-3-9600-1. Devices which pass both American and European Timings are marked as RA-3-9600.

REVISIONS

PMDATE	CN	SHT	DESCRIPTION	BY	CK	APP
			Company Confidential			
G 5/7/82	13103		REWRITTEN			

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TITLE CUSTOMER PROCUREMENT SPECIFICATION
AY-3-8914 PROGRAMMABLE SOUND GENERATOR

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED					SHEET 1 OF 19
BY							SPEC. NO. REV
DATE	4/29/82	4/29	5/1/82	5/5/82		4/29/82	CPS-10034 G

1.0 SCOPE

This Customer Procurement Specification (CPS) covers operation of the AY-3-8914 N-Channel MOS Programmable Sound Generator.

2.0 CIRCUIT FEATURES

Software control of sound generation

Interfaces to CP1600 series of 16 bit microprocessor

Three independently programmed analog outputs for frequency and amplitude

Two 8 bit general purpose input ports

Single +5 volt supply

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

4.1 FUNCTIONAL TESTING

The AY-3-8914 must be functional in a use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.5 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0eV.

4.3 IMI TEST PROCEDURE

The AY-3-8914A must be tested using IMI pattern RO-3-9505-003. The AY-3-8914 may be tested using IMI pattern RO-3-9505-003 or pattern RO-3-9504-992 and 993.

5.0 ARCHITECTURE

The AY-3-8914A is a register oriented Programmable Sound Generator (PSG). Communication between the microprocessor and the PSG is based on the concept of memory mapped input/output. Control commands are issued to the PSG by writing to these 16 memory mapped registers. Each of these 16 registers within the PSG are also readable so that the microprocessor can determine, as necessary present states as stored data values.

All functions of the PSG are controlled through its 16 registers which, once programmed, generate and sustain the sounds.

5.1 REGISTER ARRAY

The principal element of the PSG is an array of 16 control registers. These registers appear to the CPU as a block of read/write memory occupying 16 address locations of the 1024 memory space in which the PSG resides.

The PSG can be used in systems with greater than 1024 word memory space by the use of the $\overline{RWE}$ input. With this signal, the 1024 word block of memory in which the PSG resides is decoded externally and whenever a read or write to this memory space is to be carried out the $\overline{RWE}$ signal is taken low to enable the PSG.

The 10 address bits (8 bits on the data/address bus and 2 separate address bits A8 and A9) are decoded as follows:

DA0-3 These 4 low order address bits are used to select one of the internal sixteen registers.

DA4-7, A8, $\overline{A9}$ - These 6 high order address bits function as 'chip selects' and are used to position the 16 registers in the 1024 word memory space. In the deselected state the data bus is in the high impedance condition.

The address enable code for DA4-7 is mask programmable to any of the 16 possible combinations.

Input A8 and $\overline{A9}$ are enabled by a high on A8 and a low on $\overline{A9}$; all other input level combinations on these two inputs result in a deselect condition.

All addresses are held latched internally. This internally latched address is updated and modified on every 'latch address' signal presented to the PSG via the BDIR, BC2 and BC1 inputs.

The function of the sixteen registers with their address is shown on the following page:

REGISTER #$_8$	ADDRESS$_8$	FUNCTION	
R0	Base	Channel A Tone Period Fine Tune	8 Bits
R1	Base+1	Channel B Tone Period Fine Tune	8 Bits
R2	Base+2	Channel C Tone Period Fine Tune	8 Bits
R3	Base+3	Envelope Period Fine Tune	8 Bits
R4	Base+4	Channel A Tone Period Coarse Tune	4 Bits
R5	Base+5	Channel B Tone Period Course Tune	4 Bits
R6	Base+6	Channel C Tone Period Coarse Tune	4 Bits
R7	Base+7	Envelope Period Course Tune	8 Bits
R10	Base+10	Enable	6 Bits
		Bit 0 Channel A tone enable	
		Bit 1 Channel B tone enable	
		Bit 2 Channel C tone enable	
		Bit 3 Channel A noise enable	
		Bit 4 Channel B noise enable	
		Bit 5 Channel C noise enable	
R11	Base+11	Noise Period	5 Bits
R12	Base+12	Envelope Control	4 Bits
		Bit 0 Hold	
		Bit 1 Alternate	
		Bit 2 Attack	
		Bit 3 Continue	
R13	Base+13	Channel A Amplitude	5 Bits
R14	Base+14	Channel B Amplitude	5 Bits
R15	Base+15	Channel C Amplitude	5 Bits
R16	Base+16	Input Port B	8 Bits
R 17	Base+17	Input Port A	8 Bits

MEMORY MAP FOR PSG (AY-3-8914)

5.2 TONE PERIOD CONTROL

Channel A tone period is specified by registers R0 Fine Tune and R4 Course Tune

Channel B tone period is specified by registers R1 Fine Tune and R5 Course Tune

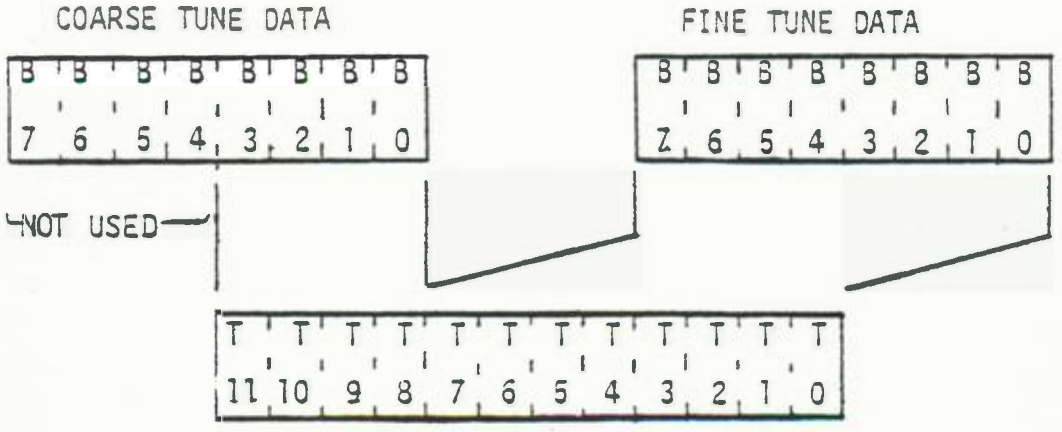
Channel C tone period is specified by registers R2 Fine Tune and R6 Course Tune

Each analog channel has associated with it two registers which specify the tone period for that channel. These two registers are the course tune data (4 bits) and the fune tune data (8 bits). Thus the tone period is defined by a 12 bit binary value, T. The base increment to this 12 bit period variable is sixteen times the period of the input clock. The tone period is given by:

$$16 \times T \times P$$

where:

P = the period of the input clock (pin 22)



12 BIT TONE GENERATOR

Note: If the Course and Fine Tune registers are both set to 000_8, the resulting period will be maximum, i.e., the generated tone period will be as if the Course Tune register was set to 017_8 and the Fine Tune register set to 377_8.

5.3 NOISE GENERATOR CONTROL

Noise is generated by a 17 bit polynomial shift register. The period of the clock to this shift register is specified by the 5 bit binary value, N, held in register R11-Noise Period. The base increment to this 5 bit period variable is sixteen times the period input clock. The shift register clock period is given by:

$$16 \times N \times P$$

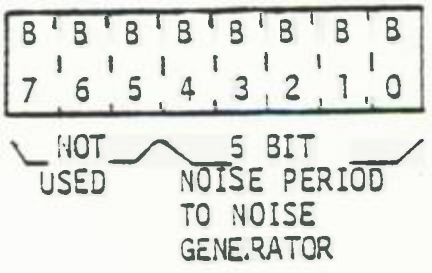
where:

P = the period of the input clock (Pin 22)

16 X N X P

where P = the period of the input clock (pin 22)

NOISE PERIOD REGISTER R11



5.4 TONE/NOISE MIXER CONTROL

The generation of tone and/or noise by the three analog channels is controlled by the Enable Register, R10.

A tone is enabled on a particular channel by writing a '0' into the tone enable bit for that channel, a '1' in that bit position will disable a tone for that channel.

Similarly, noise is enabled on an individual analog channel by writing a '0' into the noise enable bit for that channel. By writing a '1' in that bit, the noise source is disconnected from that channel.

This enables a single channel to have the following states"

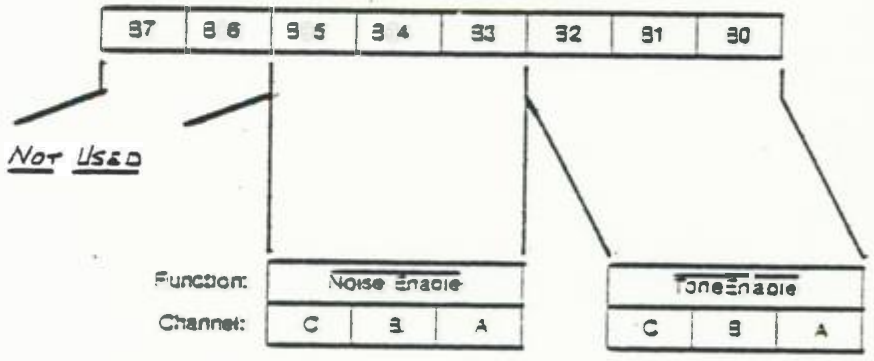
A. tone only

B. noise only

C. tone mixed with noise

D. silent, neither tone nor noise

MIXER CONTROL REGISTER - R7



Noise Enable Truth Table:

R7 Bits B5	B4	B3	Noise Enabled on Channel C	B	A
0	0	0	C	B	A
0	0	1	C	B	—
0	1	0	C	—	A
0	1	1	C	—	—
1	0	0	—	B	A
1	0	1	—	B	—
1	1	0	—	—	A
1	1	1	—	—	—

Tone Enable Truth Table:

R7 Bits B2	B1	B0	Tone Enabled on Channel C	B	A
0	0	0	C	B	A
0	0	1	C	B	—
0	1	0	C	—	A
0	1	1	C	—	—
1	0	0	—	B	A
1	0	1	—	B	—
1	1	0	—	—	A
1	1	1	—	—	—

5.5 AMPLITUDE CONTROL

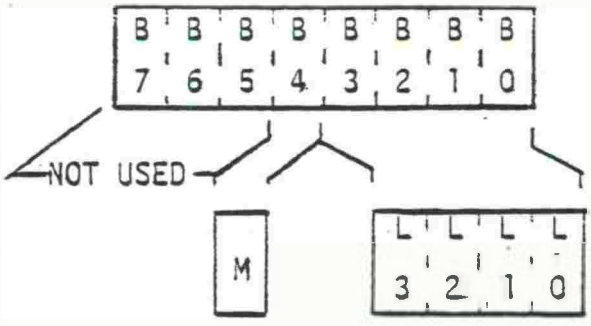
The amplitude of the signals generated on each of the three analog channels is controlled by the 5 bit Amplitude Control Register associated with that individual channel. These 5 bits are comprised of a 1 bit mode select (the 'M' bit) and a 4 bit 'fixed' amplitude level (L0-L3).

When the M bit is low at a logic '0' the output level of the analog channel is defined by the value of the 4 bit 'fixed' amplitude level of the Control Register. This amplitude level can be updated by microprocessor control thereby causing a change in the analog channel output level.

The analog outputs have sixteen possible levels.

When the M bit is high at a logic '1' the output of the analog channel is defined by the 4 bits of the envelope generator (E0-E3). The specification of the envelope generator is in section 5.6.

AMPLITUDE CONTROL REGISTER



0	0 0 0 0	AMPLITUDE DEFINED BY L0-L3
0	1 1 1 1	
1	X X X X	AMPLITUDE DEFINED BY E0-E3

5.6 ENVELOPE GENERATOR CONTROL

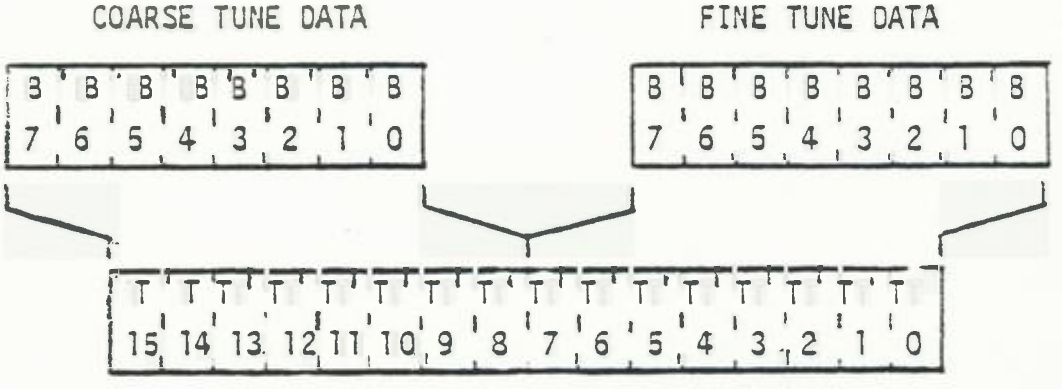
A. Envelope Period Control

The period of the sound envelope is controlled by two 8 bit registers, R4 and R7, Envelope Fine and Course Tune respectively. The 16 bit binary word, E, comprising R7 higher byte and R4 lower byte, define the number of base periods that are required to give the required envelope period. The base period has a period equal to 256 times that of the input clock. Thus, the envelope period is given by:

$$256 \times E \times P$$

where:

P = period of input clock



16 BIT ENVELOPE PERIOD GENERATOR

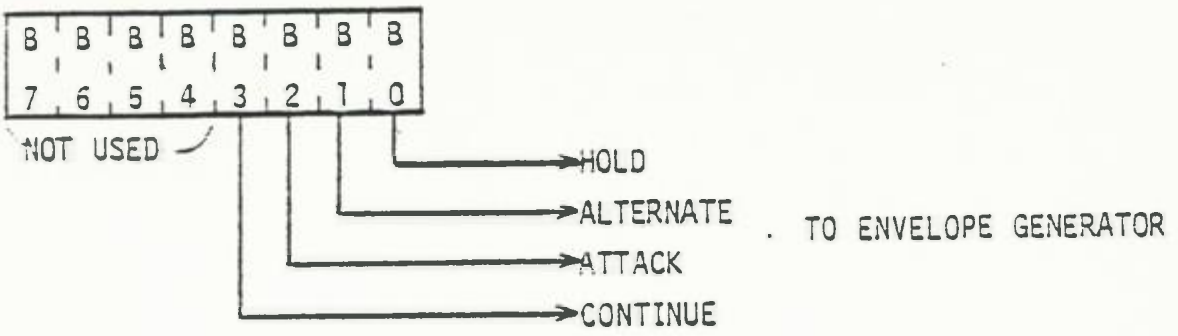
B. Envelope Shape/Cycle Control

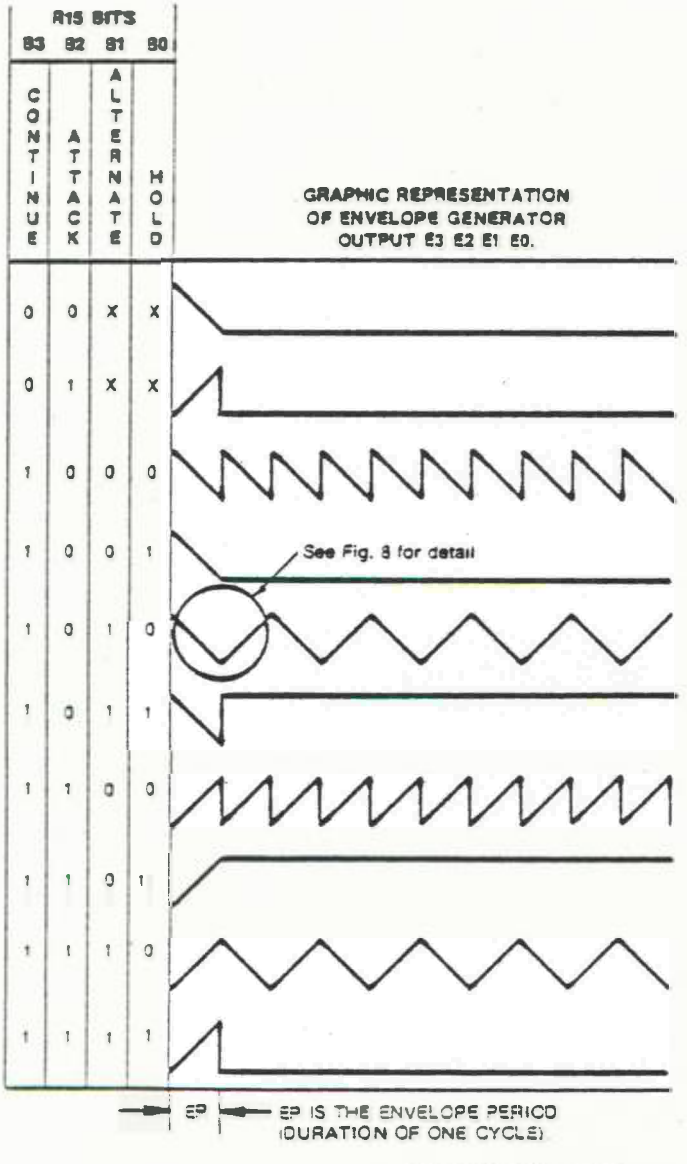
The envelope shape and cycle is controlled by register R12.

The envelope period as defined above is subdivided into sixteen timeslots to give a sixteen state per cycle envelope pattern. This pattern is given by E0-E3, the outputs of a 4 bit counter. The 4 bits of register R12 control this counter to give the desired envelope shape. The individual bits of R12 are:

Bit 0:	HOLD	When this is set high at a logic '1' the envelope is limited to one cycle, the value of the envelope at the end of the cycle being held.
Bit 1:	ALTERNATE	When set high to a logic '1' the envelope counter reverses direction at the end of each cycle (i.e., performs as an up down counter).
Bit 2:	ATTACK	When set high to a logic '1' the envelope counter will count up (attack) and when set low to a logic '0' the counter will count down (decay).

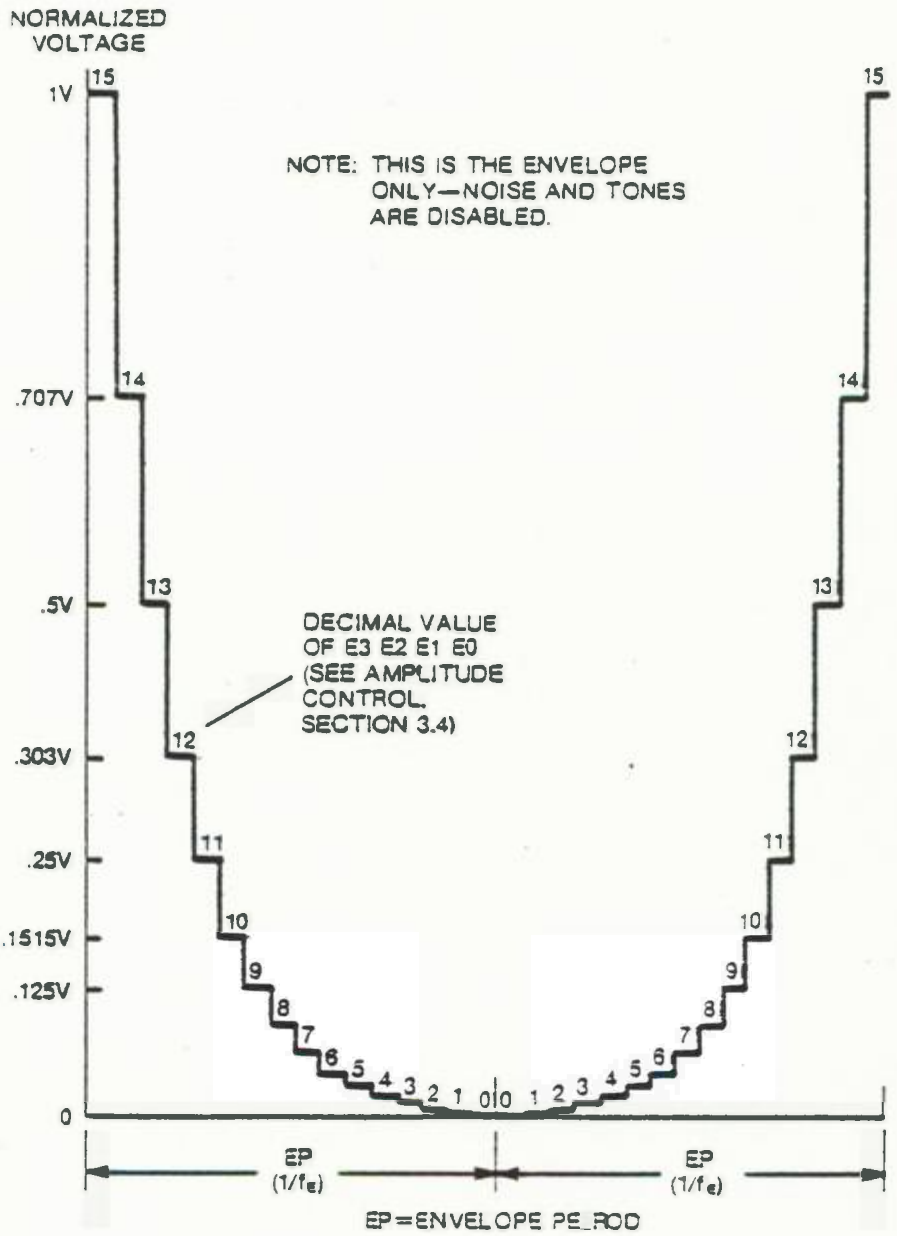
Bit 3: CONTINUE — When set high to a logic '1' the cycle pattern will be defined by the HOLD bit, and when low at a logic '0' the envelope counter will reset to E0-E3=0000 after one cycle and hold that value.


B 7
B 6
B 5
B 4
B 3
B 2
B 1
B 0
NOT USED
HOLD
ALTERNATE
ATTACK
CONTINUE
TO ENVELOPE GENERATOR


R15 BITS
B3 B2 B1 B0
CONTINUE
ATTACK
ALTERNATE
HOLD
GRAPHIC REPRESENTATION OF ENVELOPE GENERATOR OUTPUT E3 E2 E1 E0.
0 0 X X
0 1 X X
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1
See Fig. 8 for detail
EP
EP IS THE ENVELOPE PERIOD (DURATION OF ONE CYCLE)

5.7 DIGITAL TO ANALOG COUNTER

The digital to analog conversion is performed in logarithmic steps with a normalized voltage range of 0 to 1V. The specified amplitude of each converter is controlled by a 4 bit word from either the Amplitude Control Register or the Envelope Generator. The base signal of the output is the noise/tone specified for that channel.



6.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vss	-0.2V to +9.0V
Vcc with respect to Vss	-0.2V to +9.0V

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL SPECIFICATION

Ambient Temperature 0°C to +55°C

DC CHARACTERISTICS Vss = 0.0V, VCC = +4.85 to +5.15V

CHARACTERISTICS	SYM	MIN	MAX	UNITS	CONDITIONS
Input Logic Levels					
Input Logic Low	VIL	0	0.7	Volts	
Input Logic High	VOH	2.4	Vcc	Volts	
Input with Pull Ups					
A8, $\overline{\text{Reset}}$	IIL	10	100	uA	Vin = 0.0V
Inputs with Pull Downs					
$\overline{\text{A9}}$, $\overline{\text{RWE}}$	IIH	5	40	uA	Vin = 2.4V
Input with Pull Up					
A0-A7, B0-B7	IIL	15	200	uA	Vin = 0.0V
Data/Address Tri-State Leakage					
DA0-DA7(AY-3-8914)	IIL	-	200	uA	Vin = 0V:Note 1

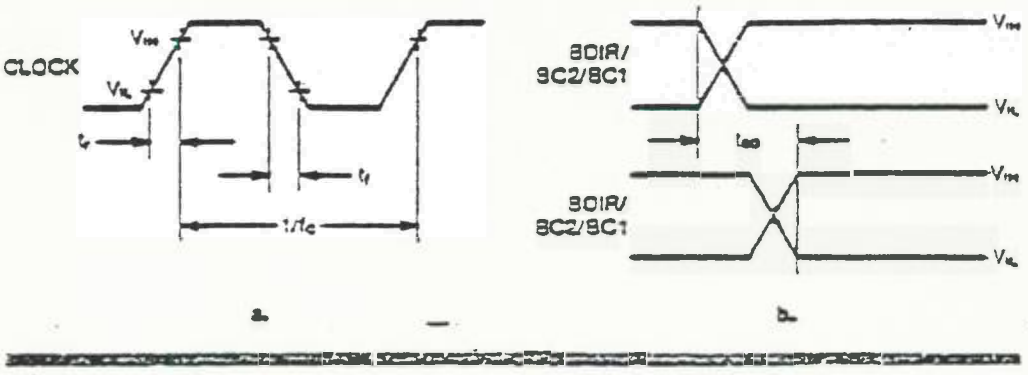
Note 1: The AY-3-8914A has a maximum of IIL of 5ua.

6.0 con't

CHARACTERISTICS	SYM	MIN	MAX	UNITS	CONDITIONS
Data Bus Output Levels DA0-DA7					
Low	VOL	0	0.5	Volts	IOL = 1.5mA] +150pf
High	VOH	2.4		Volts	IOH = 80uA]
Analog Channel Outputs					
A, B, C	-	400	2000	uA	Vout = 0.7 Amplitude control in R13, 14, 15 set to F
Power Supply					
Vcc Supply	ICC	-	75	mA	at +55°C
Clock Input					
Frequency	fc	1.79	2.0	MHz	
Rise Time	tr	-	50	nSec	- Fig. 1
Fall Time	tf	-	50	nSec	
Duty Cycle	-	40	60	%	
Bus Signals BD1R, BC1, BC2					
Skew	tbo	-	50	nSec	
$\overline{A9}$, A8, DA0-DA7 (Add. Mode)					
Address Set Up Time	tas	300		nSec	- Fig. 3
Address Hold Time	tah	65		nSec	
DA0-DA7 (Write Mode)					
Write Data Pulse Width	tdw	500		nSec	- Fig. 4
Write Data Set Up Time	tds	550	-	nSec	
Write Data Hold Time	tdh	100	-	nSec	
DA0-DA7 (Read Mode)					
Access Time from $\overline{RWE}$	tar		200	nSec	- Fig. 5
Access Time from Bus Control (BC1,BC2,BDIR)	tab		400	nSec	
Tri-State Delay	ttd		400	nSec	

CLOCK AND BUS SIGNAL TIMING:

FIG. 1



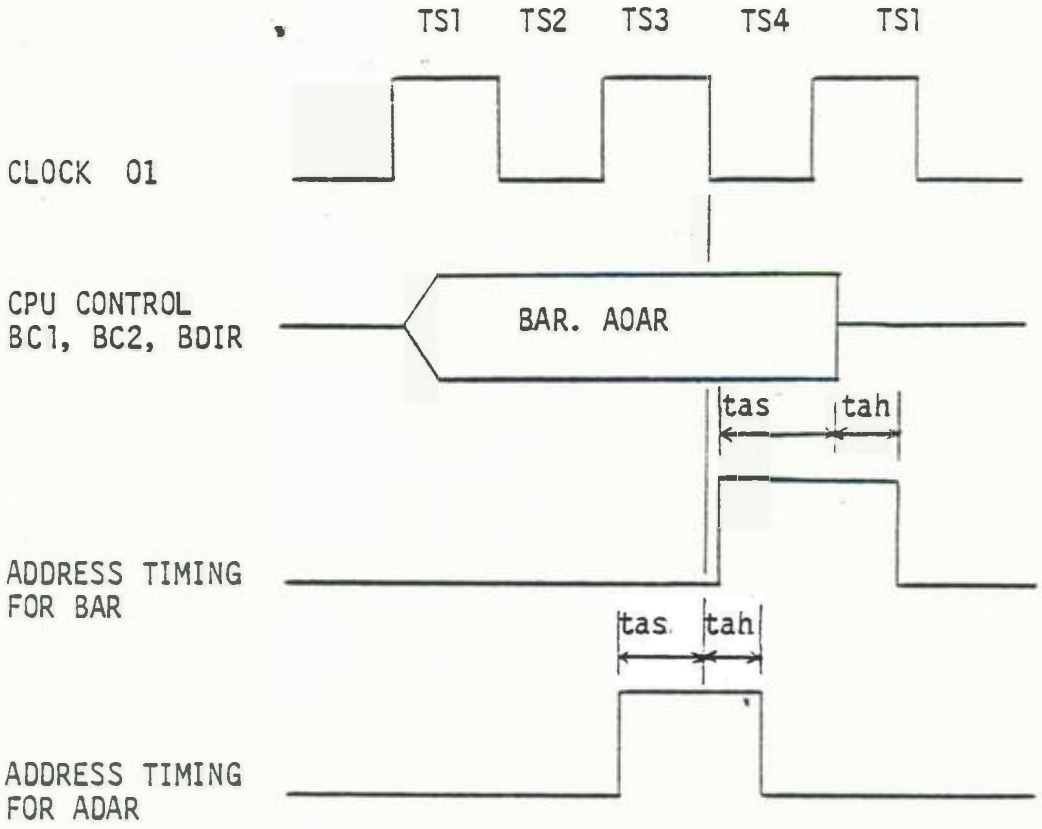


FIGURE 3 LATCH ADDRESS TIMING

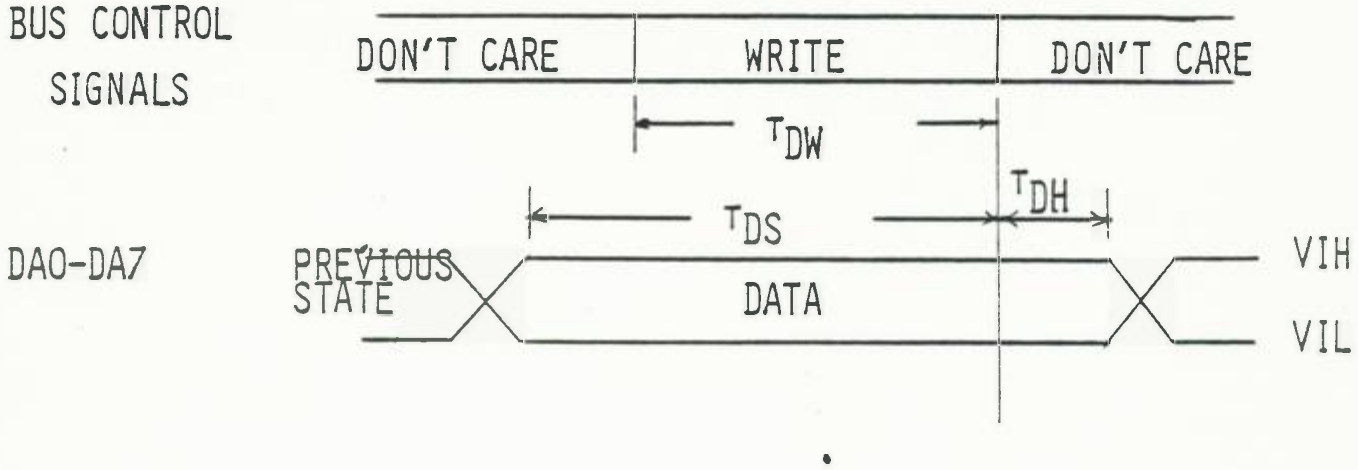


FIGURE 4 WRITE DATA TIMING

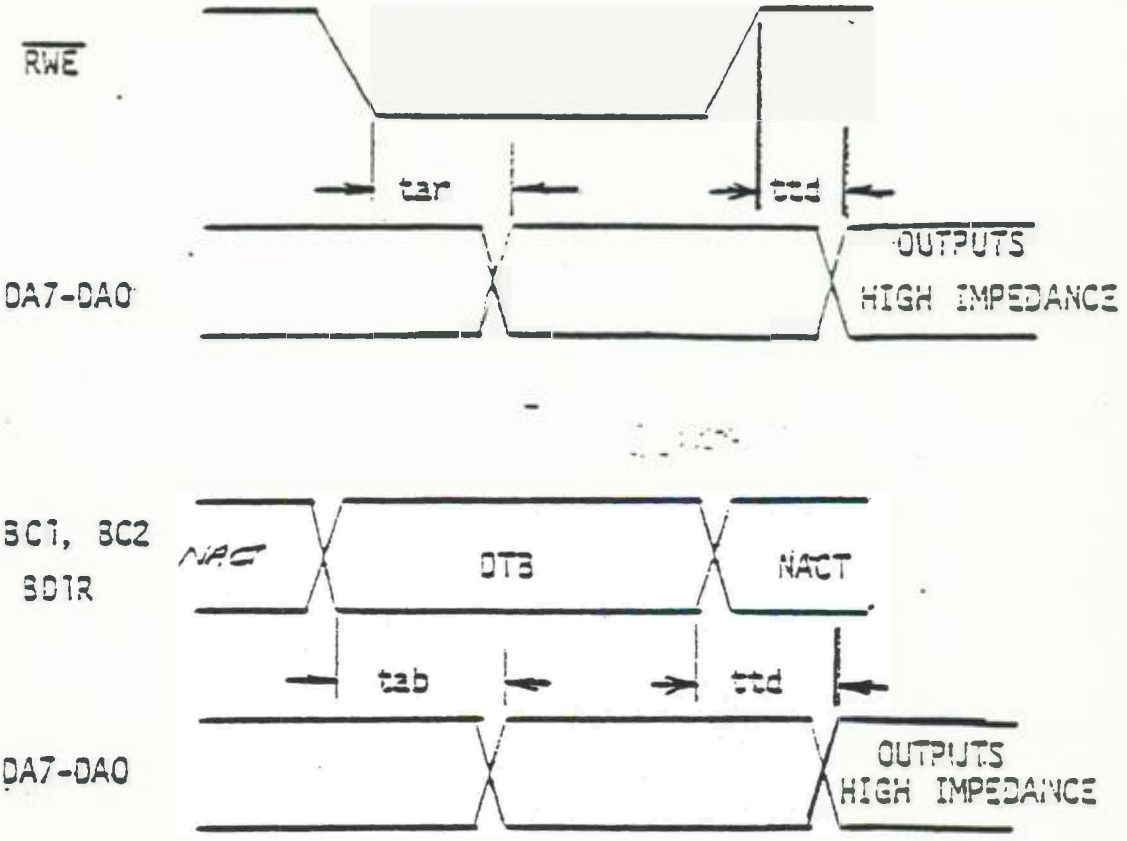

RWE
tar
ttd
OUTPUTS
DA7-DA0
HIGH IMPEDANCE
BC1, BC2
BDIR
NACT
DTB
NACT
tab
ttd
DA7-DA0
OUTPUTS
HIGH IMPEDANCE

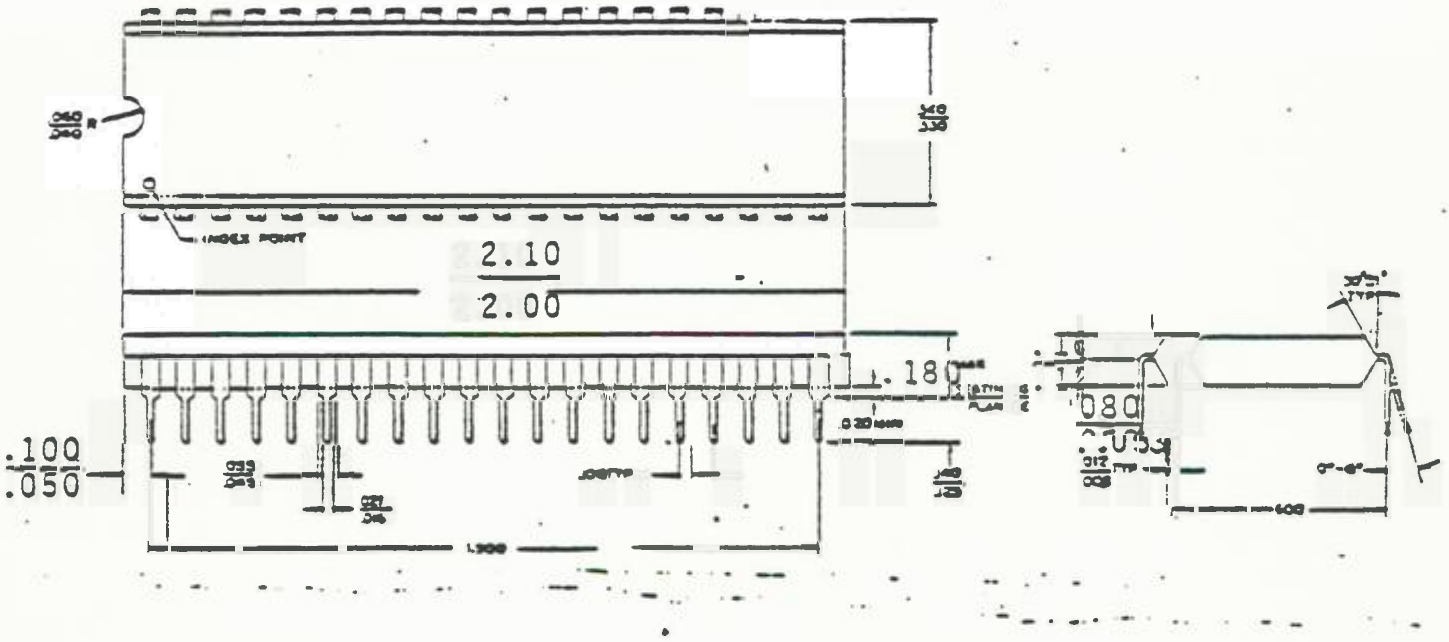
FIGURE 5

7.0 PIN FUNCTIONS

1.	Vss	21.	I/O A0 ___I/O Port A
2.	Do Not Connect (Test Input)	22.	Clock Input
3.	Analog Out Channel B	23.	$\overline{\text{Reset}}$
4.	Analog Out Channel A	24.	Do Not Connect ($\overline{\text{A9}}$)
5.	Do Not Connect	25.	Do Not Connect (A8)
6.	I/O B7	26.	$\overline{\text{RWE}}$
7.	I/O B6	27.	BDIR
8.	I/O B5	28.	BC2
9.	I/O B4	29.	BC1
10.	I/O B3 _____Input Port B	30.	DA7
11.	I/O B2	31.	DA6
12.	I/O B1	32.	DA5
13.	I/O B0	33.	DA4 Data Address Bus
14.	I/O A7	34.	DA3
15.	I/O A6	35.	DA2
16.	I/O A5 _____Input Port A	36.	DA1
17.	I/O A4	37.	DA0
18.	I/O A3	38.	Analog out Channel C
19.	I/O A2	39.	Do Not Connect (Test Output)
20.	I/O A1	40.	Vcc

8.0 MECHANICAL CHARACTERISTICS

8.1 PACKAGE DIMENSIONS



8.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
F	5/7/82	13103		REWRITTEN			

SHEET	1	2	3	4	5	6	7	8	9				
LAST REV	F	F	F	F	F	F	F	F	F				

SHEET													
LAST REV													

ISTRIBUTION LIST

SUPERSEDES

UPERSEDED BY IY IY IY IY IY IY

GENERAL INSTRUMENT | MICROELECTRONICS GROUP

TITLE Customer Procurement Specification

AY-3-8915 COLOR PROCESSOR

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED						
BY	J.D.H.	KG						
DATE	4/29/82	4.29	5/1/82	5/5/82			4/29/82	

SHEET 1 OF 9

SPEC. NO. CPS-10035

REV F

1.0 SCOPE

This Customer Procurement Specification (CPS) covers operation of the AY-3-8915 N-Channel MOS color processor circuit.

2.0 CIRCUIT FEATURES

- Operation from 7.15909MHz crystal.
- Five-line digital selection for 1 of 16 colors, blanking, Sync and color burst.
- 3.579545MHZ buffered output.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in the CPS.

4.1 FUNCTIONAL TESTING

The AY-3-8915 must be functional in a use test defined in CPS-10043 and/or CPS 10049.

5.0 CIRCUIT DESCRIPTION

The required color to be displayed for each 280 nSec PIXEL is decoded on a four line binary coded input. This selects one of sixteen possible colors. An external resistor network completes the D to A function as shown in the schematic Fig. 1 of this document. The waveform plus table illustrates the use of the five inputs to produce composite sync, color burst, line blanking, frame blanking and video.

The external video input pin provides the ability to superimpose white high resolution (140 nSec wide) video information over the picture (color image).

6.0 IMPUT CODE ASSIGNMENT — TIME SLOT (RELATIVE VOLTAGE AMPLITUDES) — COLOR OUTPUT DESCRIPTION

V5	V4	V3	V2	V1	+Q	-I	-Q	+I	
0	0	0	0	0	4	4	4	4	Color 1
0	0	0	0	1	8	12	7	1	Color 2
0	0	0	1	0	10	4	7	14	Color 3
0	0	0	1	1	10	8	12	12	Color 4
0	0	1	0	0	3	9	12	7	Color 5
0	0	1	0	1	5	11	13	8	Color 6
0	0	1	1	0	10	7	15	15	Color 7
0	0	1	1	1	13	13	13	13	Color 8
0	1	0	0	0	9	9	9	9	Color 9
0	1	0	0	1	8	13	12	7	Color 10
0	1	0	1	0	10	6	11	14	Color 11
0	1	0	1	1	9	9	5	5	Color 12
0	1	1	0	0	14	6	4	12	Color 13
0	1	1	0	1	13	13	7	7	Color 14
0	1	1	1	0	6	10	14	11	Color 15
0	1	1	1	1	12	7	4	9	Color 16
1	X	X	0	0	4	4	4	4	Blanking
1	X	X	1	0	2	2	6	6	Color Burst
1	X	X	0	1	0	0	0	0	Sync
1	1	1	1	1	0	15	0	15	Test

X = Don't Care

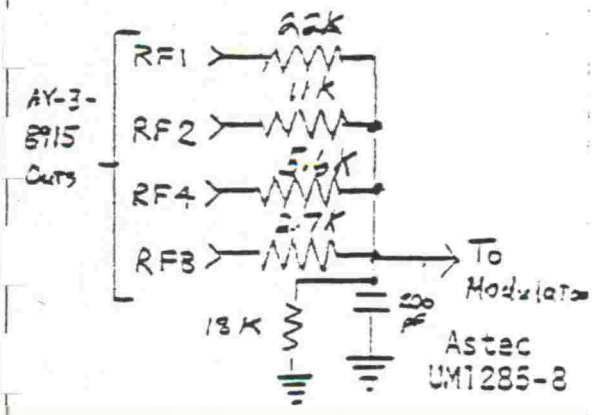


FIG. 1

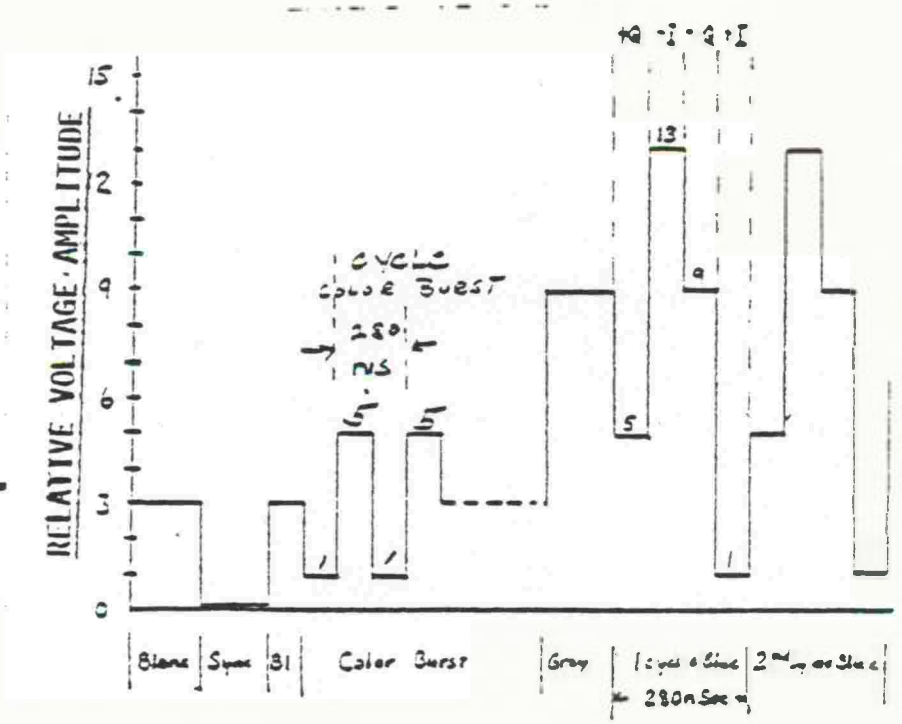


Fig. 1

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vss	-0.2v to +9.0v
Vcc with respect to Vss	-0.2v to +9.0v

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL SPECIFICATION

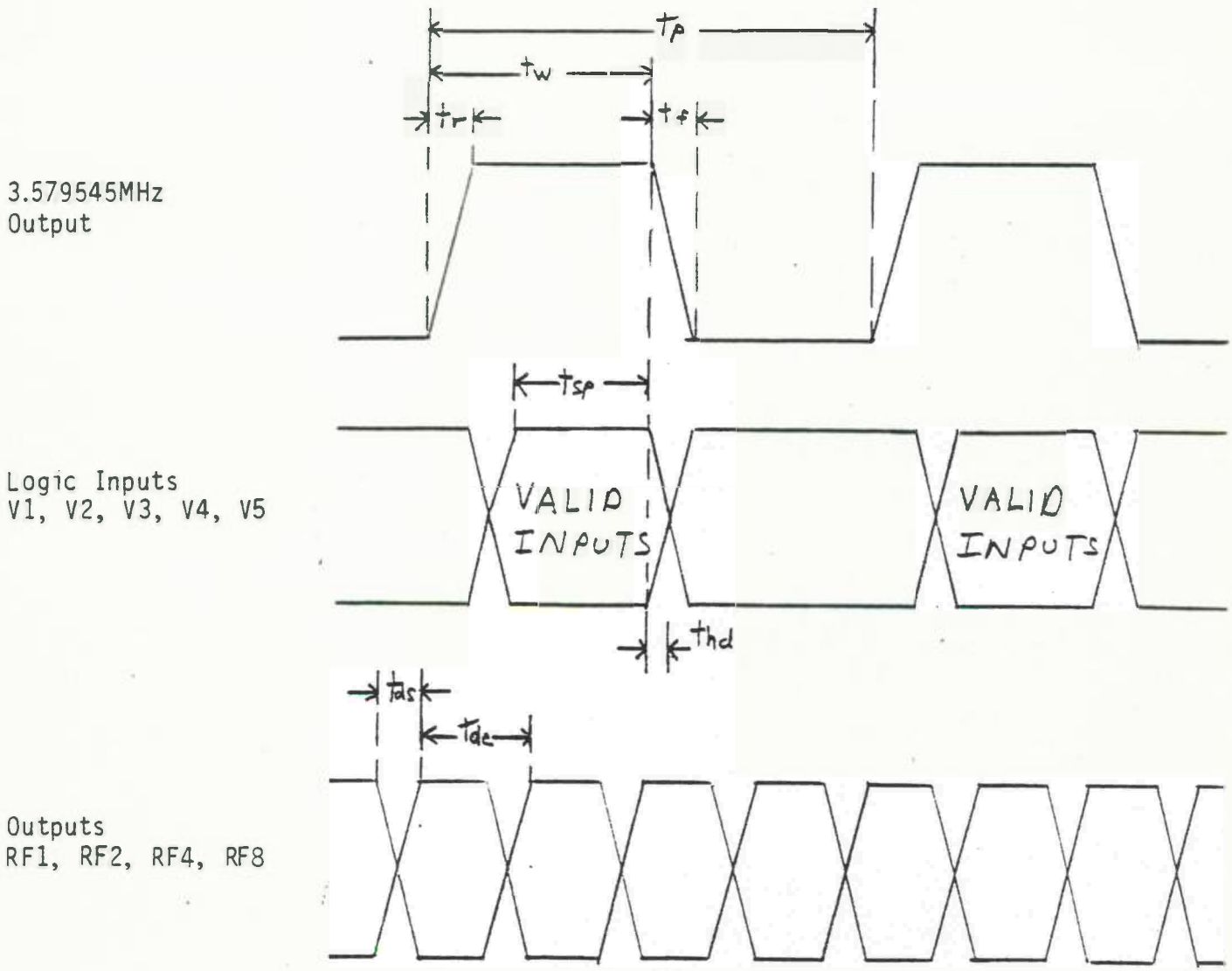
Ambient Temperature 0°C to +55°C

DC CHARACTERISTICS

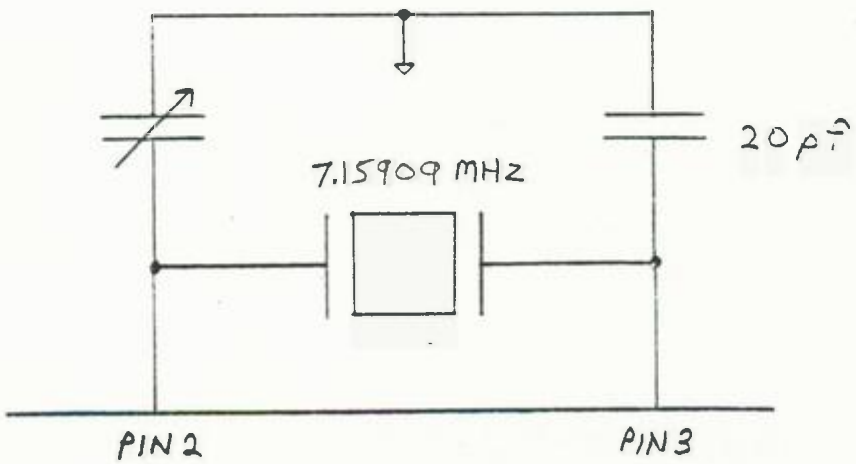
Vss=0.0V, Vcc=+4.85V to +5.15V

CHARACTERISTIC	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
3.579545 MHz Clock Output						
Output Logic Low	VOL	0	-	0.5	volts	1.5mA] +100pf
Output Logic High	VOH	2.4	-	Vcc	volts	80ua]
Logic Inputs V1, V2, V3, V4, V5, EXT. VIDEO						
Input Logic Low	VIL	0	-	0.7	volts	
Input Logic High	VIH	2.4	-	Vcc	volts	
Input Leakage Current	IIL			5	uA	0V to Vcc
Outputs RF1, RF2, RF4, RF8						
Output ON		4.0	-	-	mA	Vout=+0.5V
Output OFF		-	-	10	uA	Vout=+2.4V
Supply Current						
Vdd Supply	Icc	-	-	60	mA	at +55°C

AC CHARACTERISTICS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Input Crystal Oscillator						
Frequency	F	-	7.15909	-	MHz	7.15909 MHz Crystal Trimmed by External Capacitors
3.579545MHz Clock Output						
Rise Time	tr	-	-	30	nSec	
Fall Time	tf	-	-	25	nSec	
Pulse Width	tw	-	140	-	nSec	
Clock Period	tp	-	280	-	nSec	
Logic Inputs V1, V2, V3, V4, V5						
Set-Up Time	tsp	100	-	-	nSec	
Hold Time	thd	-	-	0	nSec	
Outputs RF1, RF2, RF4, RF8						
Data Cycle Time	tdc	-	70	-	nSec	
Data Settle Time	tds	-	-	25	nSec	



SIGNAL TIMINGS



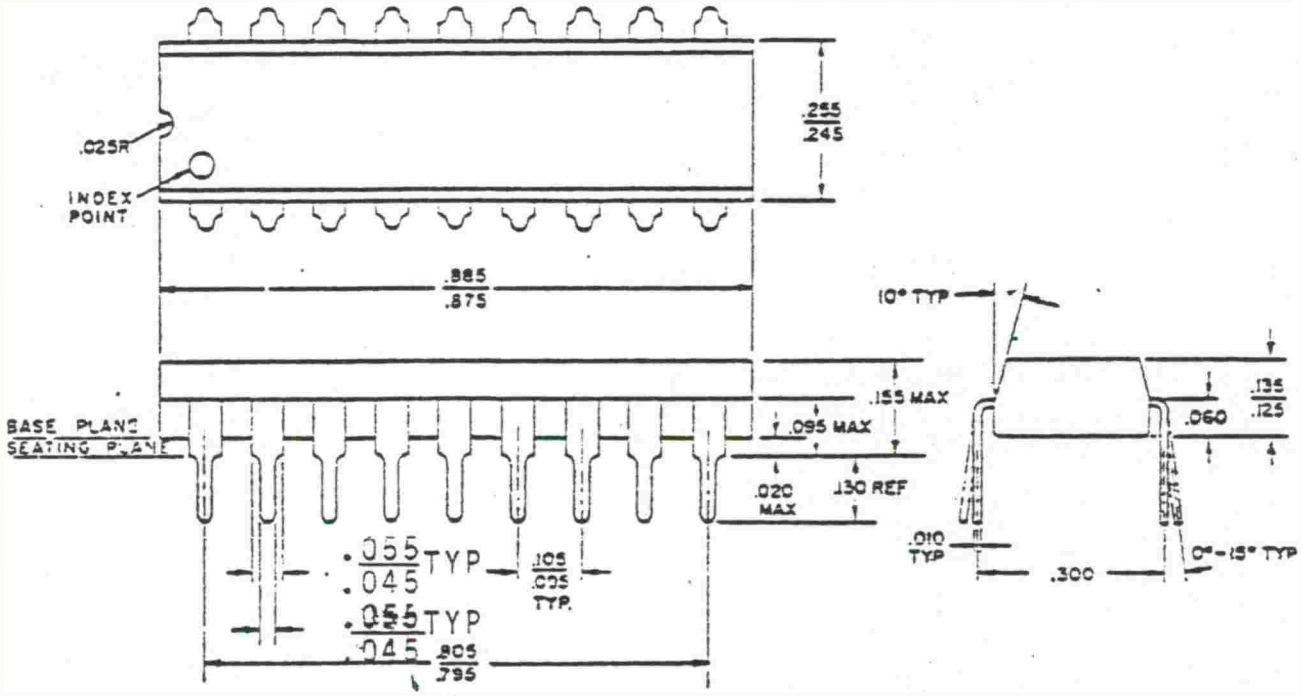
RECOMMENDED CRYSTAL CONNECTIONS

8.0 PIN ASSIGNMENT

PIN	FUNCTION
1	Vss
2	OSC In
3	OSC Out
4	V5
5	V4
6	V3
7	V2
8	V1
9	RF1
10	RF2
11	RF4
12	RF8
13	Vcc
14	Ext. Video
15	Clock (3.579545 MHz clock output)
16	No Connection
17	Test Reset (Connect to Vcc)
18	No Connection

9.0 MECHANICAL CHARACTERISTICS

9.1 PACKAGE DIMENSIONS



9.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
F	5/7/82	13108		REWRITTEN			

GI DRAWING
AND SPEC. CONTROL
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SHEET	1	2	3	4	5	6	7	8					
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SHEET													
LAST REV													

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SUPERSEDES

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GENERAL INSTRUMENT | MICROELECTRONICS GROUP

TITLE

CUSTOMER PROCUREMENT SPECIFICATION CP-1610

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED					
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
DATE	4/24/82	4/29	5/1/82	5/5/82	[illegible]	4-29-82	

SHEET 1 OF 8

SPEC. NO. CPS-10036

REV F

FORM 1E1048(8/81)

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the functional description for the General Instrument CP-1610 Microprocessor Integrated Circuit.

2.0 CIRCUIT FEATURES

Eight 16 bit general purpose registers

Four addressing modes: Indirect, direct, immediate, relative

Conditional branching on status word

16 bit 2's complement arithmetic

Status word: Carry, overflow, sign, zero

Direct memory access (DMA) for high speed data transfer

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

4.1 FUNCTIONAL TESTING

The CP-1610 must be functional in the use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.5 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0ev.

5.0 DESCRIPTION

The CP-1610 is a 16 bit, single chip, N-Channel MOS LSI microprocessor.

6.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vbb	-0.2v to +18.0v
Vcc, Vdd, Vss with respect to Vbb	-0.2v to +18.0v

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operational Specification

Ambient Temperature	0°C to +55°C

D.C. CHARACTERISTICS

Vss = 0.0V, Vcc = +4.85V to +5.15V, Vdd = +10.8V to +11.8V
Vbb = -2.1V to -2.4V

Bus Control Signals

BD1R	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, DO-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, DO-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, DO-D15 = Input
0	1	1	DTB	Data to Bus, DO-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Inputs Ø1, Ø2					
High	VIHC	10.4	12.5	Volts	
LOw I	VILC	0	0.6	Volts	
Input Current	ICL		20	mA	VIHC = 12.5 Volts
Logic Inputs					
Pins 6,7,8,9,10,11, 12,13 14,15,16,17, 18,19,20,21, 27,31	IIL	100	1200	uAmps	VIN = 0 Volts
	IIH	0	200	uAmps	VIN + 2.4 Volts
Logic Outputs DB					
LOw	VOL		0.5	Volts	IOL = 500uA] +
High	VOH	2.4		Volts	IOH = 120uA] 150pf
Control Outputs					
Pins 3,4,5,29					
LOw	VOLC		0.5	Volts	IOL = 1000uA] +
High	VOHC	3.0		Volts	IOH = 100uA] 100pf
Power Supply Current					
Vdd Supply	Idd		75	mA]	
Vcc Supply	Icc		25	mA]	at +55°C
Vbb Supply	Ibb		3	mA]	

Note: Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz.
Not measured during production test.

A.C. CHARACTERISTICS

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Pulse Inputs Ø1 Ø2					
Pulse Width	tØ1,tØ2	160		nSec	at Logic 1
Skew (Ø1,Ø2 delay)	t12,t21	0		nSec	
Clock Period	tcy	0.5	0.560	uSec	
Rise Time 0 to 1			40	nSec	
Fall Time 1 to 0			40	nSec	
BUS SIGNALS DO-D15					
Output delay from ØI (float to output)	tbo		200	nSec	IOH = 120uA, IOL = 500uA + 150 pf
Input set up time before Ø1↓	tb1	200		nSec	
Input Hold time after Ø1 ↓	tb2	100		nSec	
Bus Control Signals BC1, BC2, BDIR					
Output delay from Ø1	toc		120	nSec	IOH = 100uA +100pf VOH = 2.2V
			175	nSec	IOH = 100uA +100pf VOH = 3.0V
Skew			30	nSec	
$\overline{\text{BUSAK}}$ Output Delay from Ø1	tbu		250	nSec	

7.0 PIN ASSIGNMENTS

1	No Connection	21	DB2
2	$\overline{\text{MSYNC}}$	22	No Connection
3	BC1	23	No Connection
4	BC2	24	No Connection
5	BDIR	25	No Connection
6	DB15	26	No Connection
7	DB14	27	$\overline{\text{INTRM}}$
8	DB13	28	Connect to +5V
9	DB12	29	$\overline{\text{BUSAK}}$
10	DB11	30	No Connection
11	DB10	31	$\overline{\text{BUSRQ}}$
12	DB9	32	Connect to +5V
13	DB8	33	Connect to +5V
14	DB0	34	Vcc
15	DB1	35	Vbb
16	DB7	36	Vdd
17	DB6	37	Ø2
18	DB5	38	Ø1
19	DB4	39	Vss
20	DB3	40	Connect to +5V

CLOCK & BUS TIMING

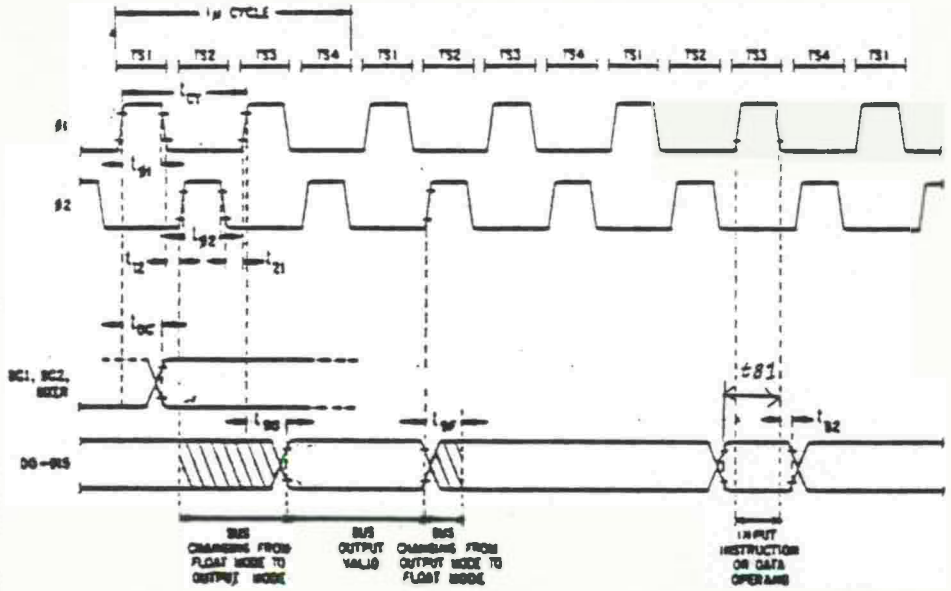


FIGURE 1

BUS ACKNOWLEDGE TIMING

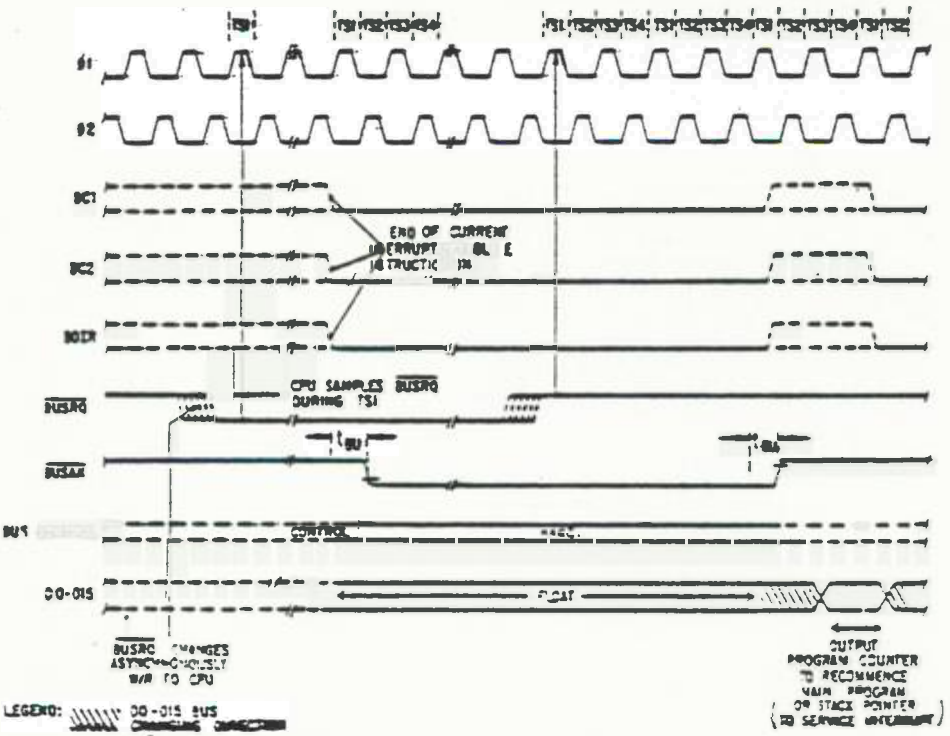
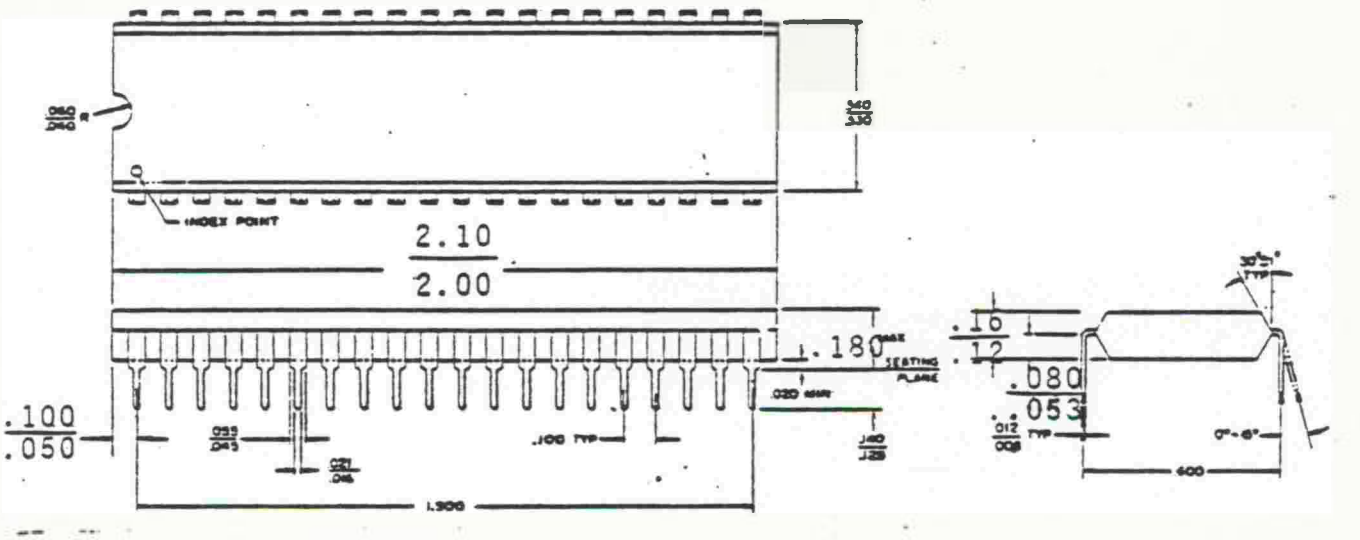


FIGURE 2

8.0 MECHANICAL CHARACTERISTICS

8.1 PACKAGE DIMENSIONS



8.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

REV SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
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SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13
LAST REV	F	F	F	F	F	F	F	F	F	F	F	F	F

SHEET	14	15	16	17	18	19	20	21 22	23 24	25 26	27 28		
LAST REV	F	F	F	F	F	F	F	F F	F F	F F	F F		

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SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT | MICROELECTRONICS GROUP

TITLE: CUSTOMER PROCUREMENT SPEC. AY-3-8900-1

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED						SHEET 1 OF 28	
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	SPEC.NO.	REV
DATE	4/29/82	4/29	5/1/82	5/5/82	[illegible]		4/29/82	CPS-10037	F

FORM 1E104(3/81)

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the functional description for the AY-3-8900-1 STIC MOS I.C.

2.0 CIRCUIT FEATURES

- o Outputs include coded signal timings for NTSC compatible video signal generation.
- o Operation from a 3.579545 MHz clock.
- o 8 coordinate addressable foreground objects on a grid of 167H by 105V of which 159 x 96 are visible positions.
- o Foreground objects independently programmable for half height, y zoom, x zoom and 8 or 16 character lines high.
- o Selectable background display on a matrix of 20 H by 12 V using 8 x 8 picture elements.
- o 16 digitally selectable colors.
- o Capable of accepting data, address and graphics information on common multiplexed bus.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit will be subjected to the electrical parameters given in the CPS.

4.1 FUNCTIONAL TESTING

The AY-3-8900-1 must be functional in a use test defined in CPS-10043.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.5 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0ev.

5.0 SYSTEM DESCRIPTION

The AY-3-8900-1 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility, which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900-1 operates within the computer system by time sharing a bi-directional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900-1 has switched to the CPU controlled mode.

SR2 is issued thirteen or fourteen times per picture frame depending on picture offset. The AY-3-8900-1 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900-1 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also issued during the CPU controlled mode in response to BAR, ADAR or DW to enable an external device on the 14 bit BUS.

The second control bus is used to specify address, read and write sequences for the area of external memory used to store the graphic character "dot" patterns. The three signals on this bus are BAR', DTB' and DWS'. The BAR' is output by the AY-3-8900-1 when a valid graphics character address is on the 14 bit bus. The external memory must latch this address for future read or write operations. The DTB' signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit bus. The DWS' signal indicates that a "write" is requested.

5.0 cont.

The graphic control bus is used during "STIC" time in the fetch of "foreground" object patterns and "background" object patterns. During the non "STIC" time when in the CPU controlled mode, the graphics control bus can be used to link the memory area containing the graphics patterns to the main memory area of the external microprocessor.

The third control bus communicates with the external CPU. This bus comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control bus is only validated if the AY-3-8900-1 is in the CPU controlled mode, otherwise it is ignored.

6.0 DATA STRUCTURES

6.1 HORIZONTAL POSITION DATA WORD

8 bits of an 11 bit word are used to control the horizontal positioning of a foreground object to a visible resolution of one part in 167.

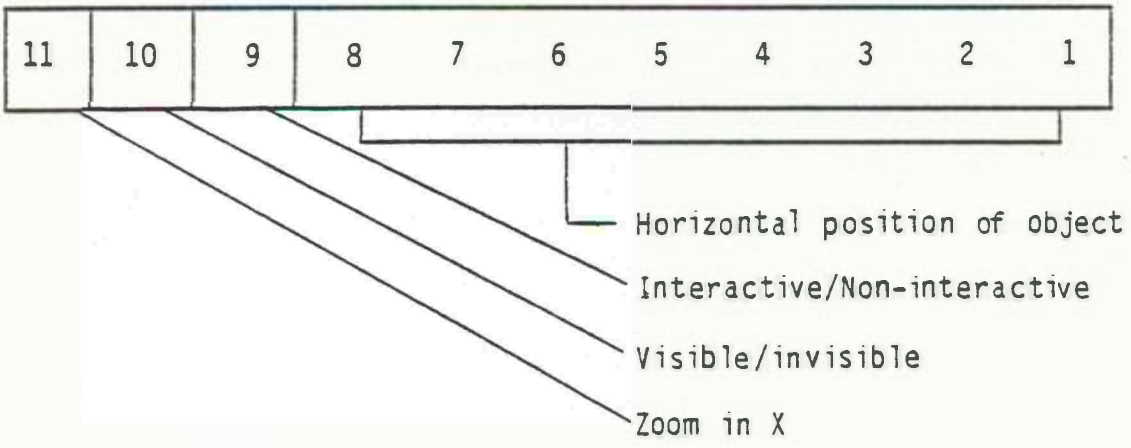
The actual X coordinate positions are 8 to 167 and the extra seven locations are used to permit objects to progressively "disappear" into the border area.

The extra seven locations are on the left hand side and effectively give a negative positioning of seven units off the screen.

The data for the objects are loaded into address locations $(0)_8$ through $(7)_8$ in STIC. The lower eight bits of the word (DB0-DB7) defines its horizontal position. The ninth bit selects whether the moving object is interactive or non-interactive. The tenth bit controls the visability.

The eleventh bit is an X zoom control which, if set to a logic 1, clocks out the object shift register at half speed which doubles the object size displayed on the screen in the X direction.

The horizontal position bits are designated as follows:



6.2 VERTICAL POSITION DATA WORD

7 bits of a 12 bit word are used to control the vertical positioning of each moving object to a resolution of one part in 104.

The actual Y coordinate positions also allow objects to disappear top or bottom and an extra eight positions are provided above the top of the active screen area.

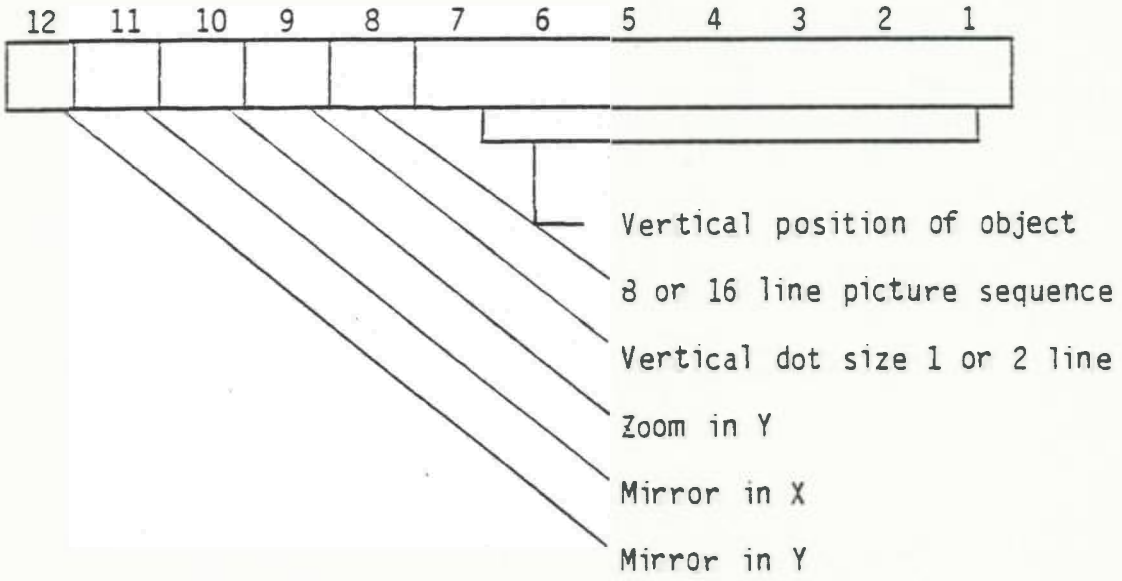
The data for the Y coordinate positions are loaded into address locations $(10)_8$ through $(17)_8$ within STIC. The lower seven bits of the word define the vertical Y position of the top edge of the object. The eighth bit allows the character to be drawn as an 8 X 8 matrix or an 8 X 16 matrix. The significance of the larger matrix is that you can have a higher resolution object by using the half height feature or it may simply be used to draw more complex shapes within the vertical rectangle. If a sixteen line picture (data changes) is required, the start position for the character address in memory must have the lower bit (DB3) at a logic zero to allow STIC to consecutively address sixteen eight-bit words. The data patterns within the memory must be organized to allow sixteen line characters to occupy two consecutive eight byte blocks within the graphics memory area. (STIC provides the lower four bit binary, current line address to memory rather than a three bit code as used in eight line pictures).

The ninth bit controls the vertical size of the minimum picture element PIXEL. Throughout the description of AY-3-8900-1 character display capabilities, the minimum picture element, PIXEL, is defined as a "square" having a timed width equal to the period of the color reference crystal, approximately 280 nSec., and a vertical height of two drawn lines on a non-interlaced 262 line half frame. The "foreground" or "moving" objects have a half height control which allows a pattern change on all drawn lines instead of every second line, and this reduces the minimum PIXEL to 280 nSec by one drawn line. The ninth bit control, if set to a logic 1, causes the corresponding moving object to be drawn over eight video lines instead of the normal sixteen lines, assuming the bit 10 is at a logical "0".

6.2 cont.

The eleventh and twelfth bits respectively control the X and Y mirror. The tenth bit controls Y zoom and operates in a binary manner with the 1 or 2 line select bit to provide a vertical selection of 1, 2, 4, or 8 drawn lines before a data change. The maximum height object would be sixteen data lines times 8 which is 128 visible lines.

The vertical position bits are designated as follows:



BIT 10	BIT 9	
0	0	Data change each line
0	1	Data change every two lines
1	0	Data change every four lines
1	1	Data change every eight lines

6.3 FOREGROUND OBJECT IDENTIFICATION AND CONTROL

Locations $(20)_8$ through $(27)_8$ within STIC store the object library address bits and the color and control information for the eight foreground objects. The lower three bits select 1 of the first 8 available colors. The next 9 bits define the character start address from a library of 512 possible characters. The thirteenth bit operates in conjunction with the three color bits to give a 1 from 16 color selection. The fourteenth bit controls the display priority of that particular foreground object relative to the background. A logic zero in this bit allows the foreground object color to replace any background character where there is an overlap of the drawn image. The foreground objects themselves have a related priority in that a lower numerical object has a higher visible priority that a higher numerical object, i.e, object zero takes precedence over all other objects, object one covers all except zero, etc. The priority draw is conditional upon the object being visible. If an invisible object has been programmed it can be interactive with all other objects but it will not enter the priority draw logic. This stops invisible foreground objects from producing a 'negative' effect if it has a priority over any background character which it may overlap.

The effect of priority defines which object should control the color display on areas which overlap. Because the priority may be changed on any frame, this may be used by the programmer to produce a three dimensional effect of objects being in front of some background displays and behind others. The identification and control words are designated as follows:

14	13	12	11	10	9	8	7	6	5	4	3	2	1
MK1	MK2	CHARACTER START ADDRESS									C2	C1	C 0

BIT	FUNCTION	LOGIC 0	LOGIC 1
MK1	Priority Control	Foreground	Background
MK2	Color Control	Group A	Group A and B

6.4 FOREGROUND OBJECT COMPUTER CONTROL

The CPU must accept the 8900 STIC in its memory map of 0_8 to 77_8. In general most words or bits are read/write but there are some exceptions. The bit controlling the CPU release of the 14 bit bus called 'Special Bit', is write only to the CPU. The interaction words at $(30)_8$ to $(37)_8$ are set by the STIC and can set or be reset by the CPU.

There are three words controlling each of the eight foreground objects, an X coordinate, a Y coordinate and an object descriptor.

6.5 FOREGROUND OBJECT INTERACTION

Moving Objects - During display of the active picture, all interactive objects are optionally inspected for overlap with other interactive objects. An "overlap" is defined such that a logic 1 or active area of one object is overlapped on a logic 1 of any other object. Either or both objects may be invisible.

If an overlap is detected, the hit signal is stored in an eight word array positioned at addresses $(30)_8$ to $(37)_8$ within STIC. The array is organized as eight by ten bit words and the lower byte is assigned a matrix with significance relative to the numerical value of the object. Word zero, bit zero is used for object zero, bit one for object zero overlapping with object one, etc. The bits for an object interacting with itself are wired to a permanent zero and cannot be set by the CPU.

	BR	BO	7	6	5	4	3	2	1	0
Object 0	0	0	0	0	1	0	0	0	1	0
1	0	1	0	0	0	0	1	0	0	1
2	1	0	0	0	1	0	0	0	0	0
3	0	0	0	0	0	0	0	0	1	0
4	0	1	0	1	1	0	0	0	0	0
5	0	0	1	0	0	1	0	1	0	1
6	0	0	0	0	0	1	0	0	0	0
7	0	0	0	0	1	0	0	0	0	0

BD - Background Character

BR - Border

Above is a possible pattern within the interaction matrix.

Background Objects - bit nine of the interaction matrix is used to indicate if a foreground object overlapped any background object. A background object is defined as a character pattern drawn in the background mode or any color which is not white if drawn in the colored squares mode.

Border - The eight foreground objects are inspected against a border "window", and if an interactive character is overlapping the edge of this "window" the tenth bit of the Interaction Word will be set to a logic one.

6.6 COMPUTER CONTROL OF INTERACTIONS

The interaction record area of STIC is set by any shape overlap if the appropriate interaction bit has been set. The STIC gives control to the CPU from the start of an interrupt period by issuing SR1. At this time the CPU can inspect interactions and perform the normal timed object movement. The STIC is not completely disabled at this time and it still allows the CPU to pass data to and from the graphics memory area using STIC logic for timing and control signals. There is a location within STIC at address 40_8 which is the CPU-STIC control known as Special Bit. This location may be reset to a logic zero by writing from the CPU, and this must occur during the next 3.5 mSec, if the next frame is to be drawn by STIC. If the interaction matrix has not been cleared prior to the STICK being allowed to display a new frame, any new interactions will OR with the old data.

6.7 BACKGROUND OBJECTS

The background display of the STIC system is organized into a matrix of twenty horizontal positions by twelve vertical positions for a total of 240 locations. The 240 selection words are accessed in sequence from external memory.

Each "card" location on the screen is defined completely by a 14 bit word. The three least significant bits defined 1 of 8 colors for the object to be displayed and is used on conjunction with control bit BK2 (DB12) to produce a total choice of 1 of 16 colors. The next nine bits define the character start address from an external library of 512 characters. The individual rows within a character are read automatically by the 8900-1 using a Y0, Y1, Y2 three line connection.

The top three bits of the word (DB11, DB12, DB13) are control bits which describe some extra features available during the background display. There are three modes under which these codes can be interpreted. Two of these operate on the background color wash and the third code specifies the colored squares mode. These modes are explained in greater detail under a separate heading.

The drawing sequence for background characters is defined by timing logic within the 8900-1 and control logic within the system RAM. The system is synchronized by the SR1 (interrupt) signal from the STIC, which is a negative going edge generated one line after the end of active picture.

6.7 cont.

The CPU accepts this signal as an interrupt request and in sequence it will issue an acknowledge, INTAK, on the control bus, BC1, BC2, BDIR. The INTAK is decoded by the STIC and used to clock SR1 back to a logic one condition.

The timing of the background data fetch is synchronized with SR2 and SR3. The first SR2 signals the start of STIC time to the 9600. Subsequent SR2s indicate that a new row of characters has been requested by the 8900-1. SR3 is pulsed positive to request each individual character descriptor.

6.8 BACKGROUND MOTION

The entire background field may be moved by programming horizontal and vertical offset words which are located at address 60_8 for X and 61_8 for Y. These words are of three bits and they are used to provide an offset of the picture origin by an amount of up to eight counts in X and Y.

The non-offset condition is 0, 0 in the two stores and as the numbers are increased, the "picture" origin will correspondingly move right and down. To remove the effect of a "wrap around" display where half an object is at the top and half at the bottom, or left and right as the case may be, there are two control bits located at address 62_8. Bit zero set to a one effectively extends the left hand border to cover the first column of cards and correspondinbly bit one is used to extend the top border to cover the first row. For all conditions other than 0, 0 in the offset words, there will still be a 20 X 12 card display with fractional cards around the periphery. The X and Y offset and their control bits are completely independent and may be used in any combination.

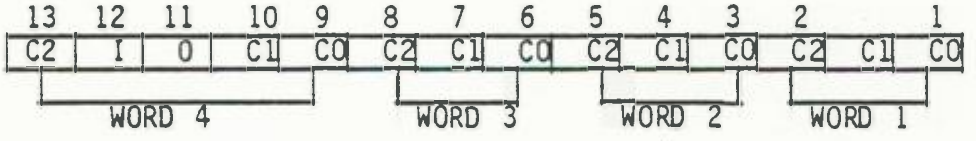
Note that the origin for the background display and the foreground positions are locked together and that a moving background will also move the foreground.

6.9 COLORED SQUARES MODE

To extend the universal application of the 8900-1, an extra capability is provided for more color programmability than the basic one object on one card approach.

This extra mode is colored squares and it operates by taking an individual 8 X 8 card and redefining it as four 4 X 4 squares. Each of the 4 X 4 squares can be programmed separately to one of seven colors (from Group A). If all the background matrix was selected in colored squares mode, this would provide an array of 40 X 24 where each of the 960 squares are separately programmed for color.

The colored square word is designated as follows:



The three color bits of each of the four words directly defines the color inside the corresponding square. The condition of three ones which would be a white square, is trapped by the display logic and the current background color is drawn in that square.

1	2
3	4

7.0 BACKGROUND COLOR

There are two modes available which provide control of the background color wash. The particular mode selected is defined by the CPU writing or reading address 41_8 within the 8900-1. The background color wash mode throughout any particular frame of 240 cards can only be changed during the CPU interrupt time initiated by SR1.

Mode 1 - If address 41_8 is read by the CPU, the 8900-1 will operate in the first background mode. This mode uses a four word, four bit cyclic stack and a stack pointer. The four words are positioned at 50_8 - 53_8 on DB0 - DB3 inclusive, and may be accessed by the CPU during the interrupt period following SR1. The stack pointer is controlled by BK1 and a logic zero will leave the pointer at its current position, a logic one will step the pointer to the next position. The stack is a continuous loop and will carry around the end position. When the pointer is incremented the new color wash will appear on the card which caused the increment.

7.0 cont.

The use of the colored squared code in any "card" position inhibits the action of BK1 and redefines it as the C2 control bit, thereby holding the stack pointer at its current position.

The pointer is reset to the top of the stack at the end of active picture.

Mode 2 - If address 41_8 is written to by the CPU, the 8900-1 will operate in the second background mode. The 14 bit word is now coded to contain program information for both the background character color and the color wash behind that character. This allows the programmer to define a colored "object" on a colored card effect with complete control of and random color changes necessary.

The recording of the background descriptor to add the background color wash reduces the character address word to six bits, allowing two further bits for use in color coding. The three bits of background control, BK1, BK2, and BK3 are also redefined.

7.0 cont.

BACKGROUND MODES:

MOOE 1:

BK1	BK2	9 BIT CHARACTER ADDRESS	C2	C1	C0

BK1	BK2	BK3	COLOR STACK POINTER
0	0	X	Group A - Current
1	0	X	Group A - Next
0	1	X	Group B - Current
1	1	X	Group B - Next
X	1	0	
X	1	0	COLORED SQUARES
DB13	DB12	DB11	

COLORED STACK

COLOR STACK POINTER

A/B	C2	C1	C0
A/B	C2	C1	C0
A/B	C2	C1	C0
A/B	C2	C1	C0

MODE 2:

C2	BK2	BK3	C1	C0	6 BIT CHARACTER ADDRESS	C2	C1	C0

C2, C1, C0 - color code for background wash

BK2 - A/B control bit, operates on color wash and not on character color for mode two.

A logic zero selects first option, logic one selects second.

7.1 BORDER COLOR

The active area of the display is surrounded by a colored border. The border may be drawn in any of the sixteen colors, and it may be programmed by the CPU via a four bit store at address 54_8, which is adjacent to the background color storage. The border color is programmed during the interrupt period following SR1 and it may be changed in any frame.

8.0 STIC TIMING

The basic timing of the device can be segregated into three operating areas. These areas are directly related to the real time raster scan operation of a domestic television receiver.

The areas are:

1. Active drawn line
2. Active line retrace
3. Vertical retrace period

1. The Active Drawn Line defines the period when a row of selectable dots are being drawn on the television screen. During this time a single video line from a row of "background" characters is drawn, using the control signals SR2, SR3, BAR', DTB' and data from an area of external memory.

   The visible dot patterns for a "foreground" object are also output at this time.

2. The Active Line Retrace is the period when the dot pattern for the individual "foreground objects are fetched from external memory. The control signals which are active at this time are BAR' and DTB'.

3. The Vertical Retrace Period extends from the last line at the bottom of the active picture until a period two lines before the restart of the active picture. The AY-3-8900-1 indicates the start of the retrace operation by issuing a negative pulse on SR1. This pulse is used by the external CPU as an indication that the STIC has finished drawing a picture. At the end of the vertical retrace period the CPU will lose access to the memory area contained within the 8900-1 chip, if special bit has been set. To allow the CPU to access memory on the 14 bit bus the 8900-1 chip operates so that the three lines SDO, SO1, SO2 and YO, Y1 and Y2 can copy bi-directional, under control of the CPU BUS BC1, BC2, BDIR.

9.0 ELECRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vbb	-0.2V to +9.0V
Vcc, Vdd & Vss with respect to Vbb	-0.2V to +9.0V

*NOTE:

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For definition of control signal codes on BC1, BC2, BDIR, please refer to sheet 3 CPS-10036.

OPERATIONAL SPECIFICATION

Ambient Temperature 0°C to +55°C

D.C. CHARACTERISTICS

Vss = 0.0V, Vcc = 5.45V to 5.95V, Vbb = -2.1V to -2.4V

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Bus Inputs					
SD0-SD13, Y0-Y3					
Logic Low	VIL		0.7	Volts	
Logic High	VIH	2.4		Volts	
Leakage	IIL		5	uA	VIN = 0V to Vcc
Bus Outputs					
SD0-SD13, Y0-Y3					
Logic Low	VOL	0	0.5	Volts	IOL = 100uA +100pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA
Control Inputs					
BC1, BC2, BDIR, RSTIN, CLOCK					
Logic Low	VIL		0.7	Volts	
Logic High	VIL	2.4		Volts	
Leakage	IIL		5	uA	VIN = 0V to Vcc
Control Ouputs					
SR1, SR2, $\overline{\text{MSYNC}}$					
Logic Low	VOL		0.5	Volts	IOL = 500uA] +100pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
BAR[1], DTB[1], DWS[1]					
Logic Low	VOL		0.5	Volts	IOL = 100uA] +50pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
SR3					
Logic Low	VOL		0.5	Volts	IOL = 100uA] +50pf
Logic High	VOH	3.0	Vcc	Volts	IOH = 100uA]

D.C. CHARACTERISTICS (cont.)

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Outputs					
Ø1, Ø2					
Logic Low	VOL		0.5	Volts	IOL = 1mA] +100pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
Power Supply Current					
Vcc	Icc		170	mA	at +55°C
Vbb	Ibb		3	mA	

Note: Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz.
Not measured during production test.

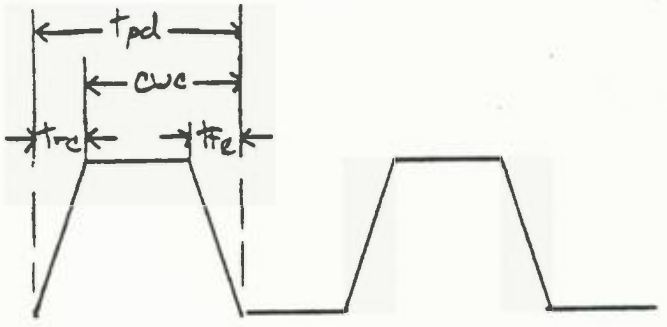
A.C. CHARACTERISTICS

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Input Freq.	fc	-	-	MHz	3.579545 externally
Rise Time	trc		30	nSec	adjusted
Fall Time	tfc		20	nSec	
Pulse Width	cwc	100	130	nSec	
CPU Time					
Data Bus (input) SD0-SD13					
Address Set Up	tas	150		nSec	
Address Overlap	tao	30		nSec	
Write Set Up	tws	400		nSec	
Write Overlap	two	200		nSec	
SD0-SD2 to Y0-Y2 bus copy	tdy		125	nSec	Data valid at start of copy
Data Bus (output) SD0-SD13					
Turn On Delay	tda*				
Turn Off Delay	tdo*				
Y0-Y2 to SD0-SD2 bus copy	tyd		200	nSec	Data valid at start of copy
BC1, BC2, BDIR Setup	tcs	0		nSec	
BC1, BC2, BDIR Overlap	tco	250		nSec	

*For a BAR or ADAR within the STIC or GRAPHICS memory address the STIC will perform a look-ahead READ immediately after the valid address. The following DTB signal is only used to disable the READ sequence at the appropriate time. If a WRITE sequence is detected the look-ahead READ is disabled in DW time and a valid WRITE procedure is completed during DWS.

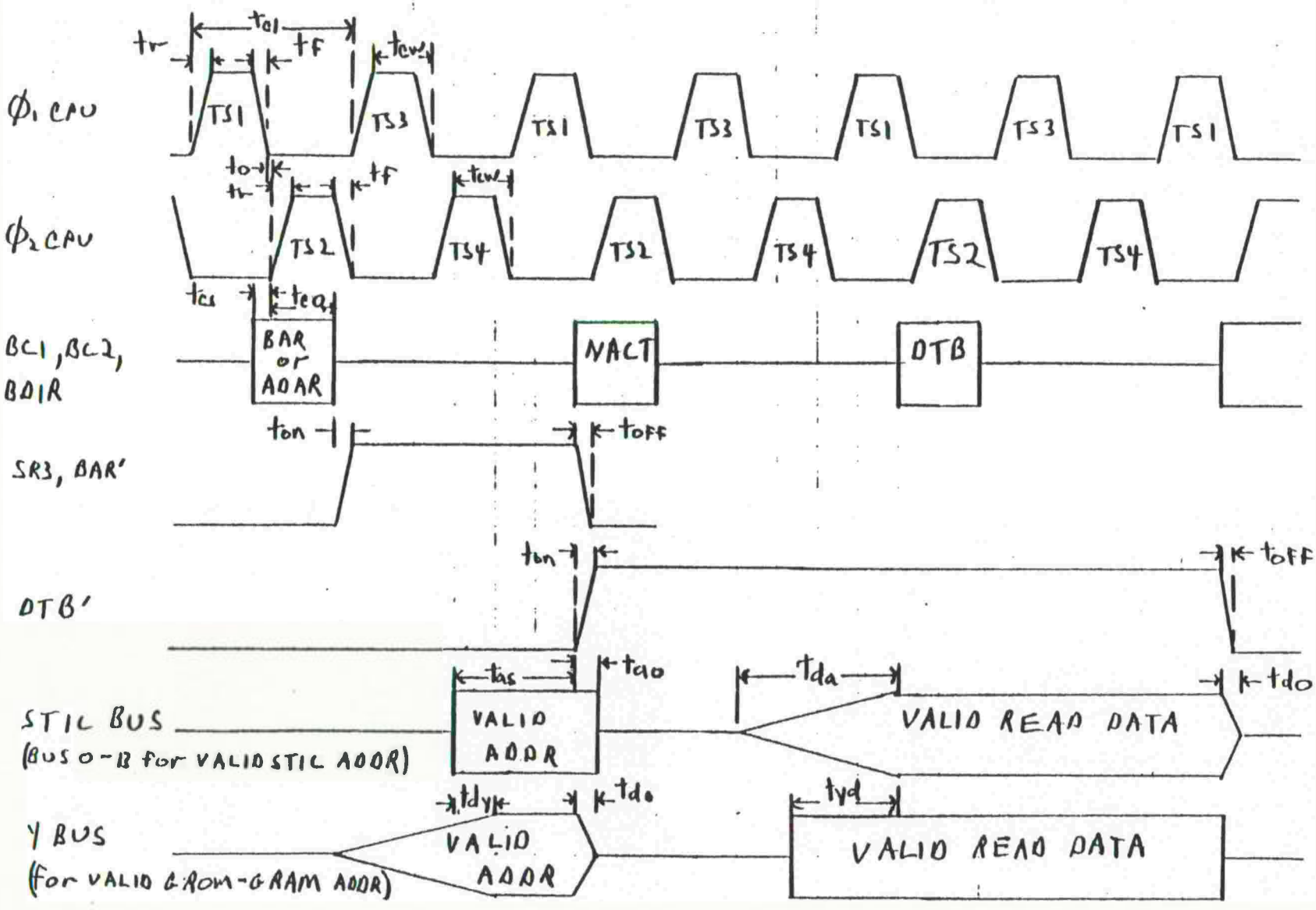
Clock Outputs Ø1, Ø2					
Rise Time	tr		40	nSec	
Fall Time	tf		30	nSec	
Overlap	to	0		nSec	
Pulse Width	tcw	170		nSec	
Control Turn On SR3, BAR[1], DTB[1] DWS[1]	ton		40	nSec	
Turn Off	toff		40	nSec	

STIC TIME	MIN	MAX	UNITS
Background Period			
Control Signals			
SR3 Turn On 0		40	nSec
SR3 Turn Off 0		40	nSec
BAR[1], DTB[1], Turn On 0		40	nSec
BAR[1], DTB[1], Turn Off 0		40	nSec
Y Bus Drive Ø ↓		250	nSec
Graphics Bus Read			
Set Up DTB[1] ↓		200	nSec
Hold DTB[1] ↓	0		nSec
Foreground Period			
SB and Y Bus Drive Ø↓		250	nSec
SB and Y Bus Hold Ø ↓	0		nSec
Graphics Bus Read			
Set Up DTB[1] ↓		200	nSec
Hold DTB[1] ↓	0		nSec

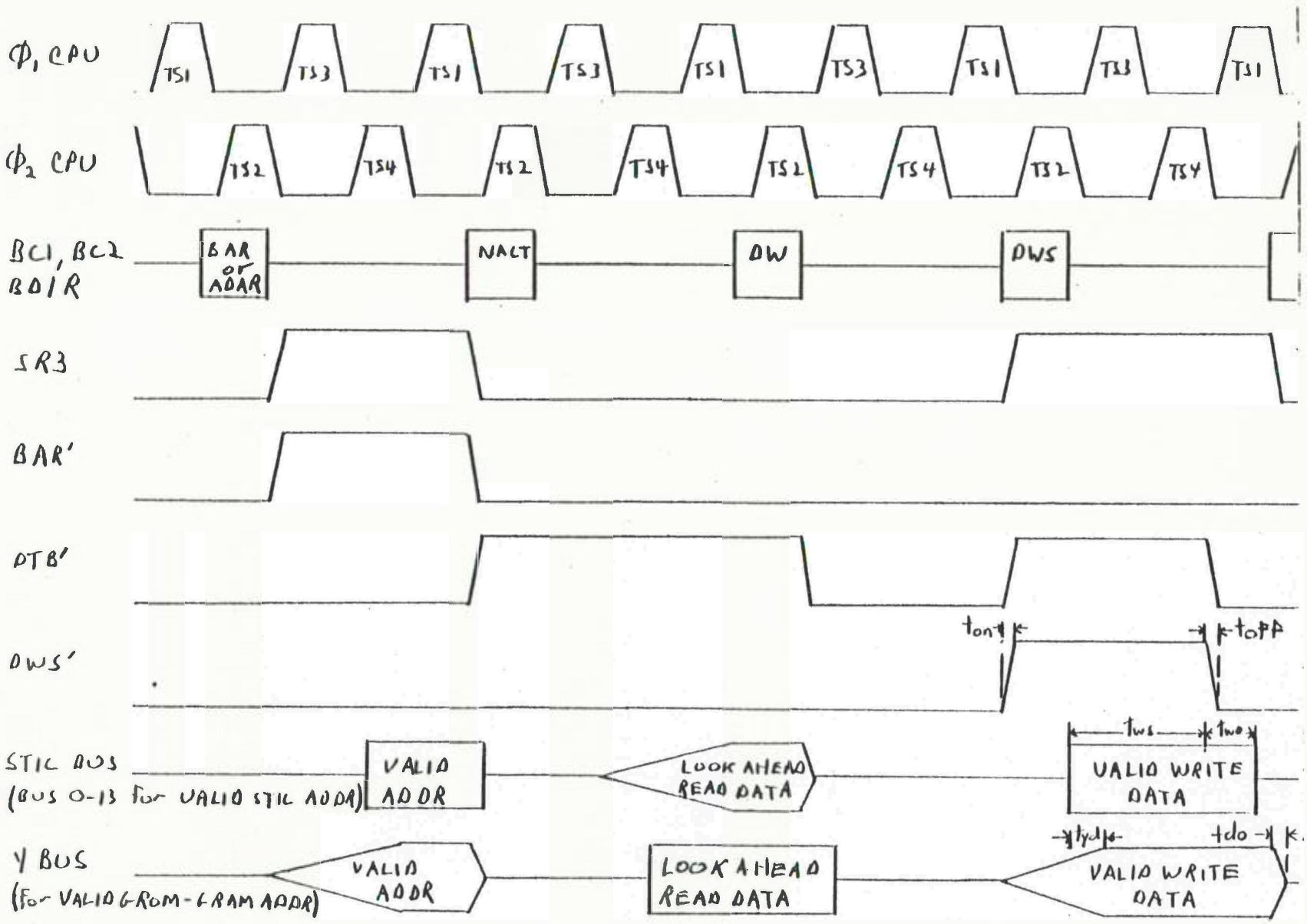


STIC INPUT

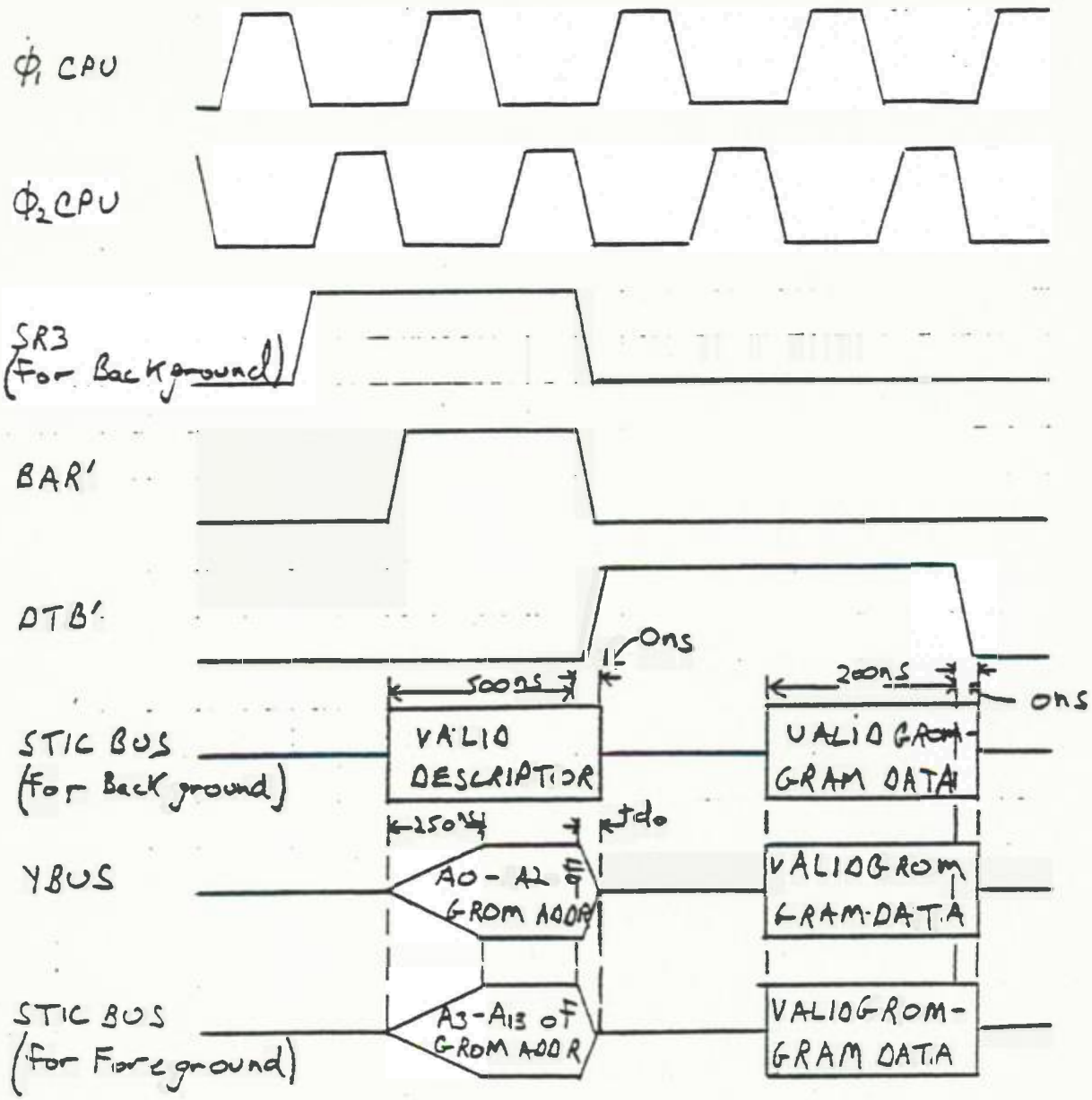
CLOCK



CPU TIME READ

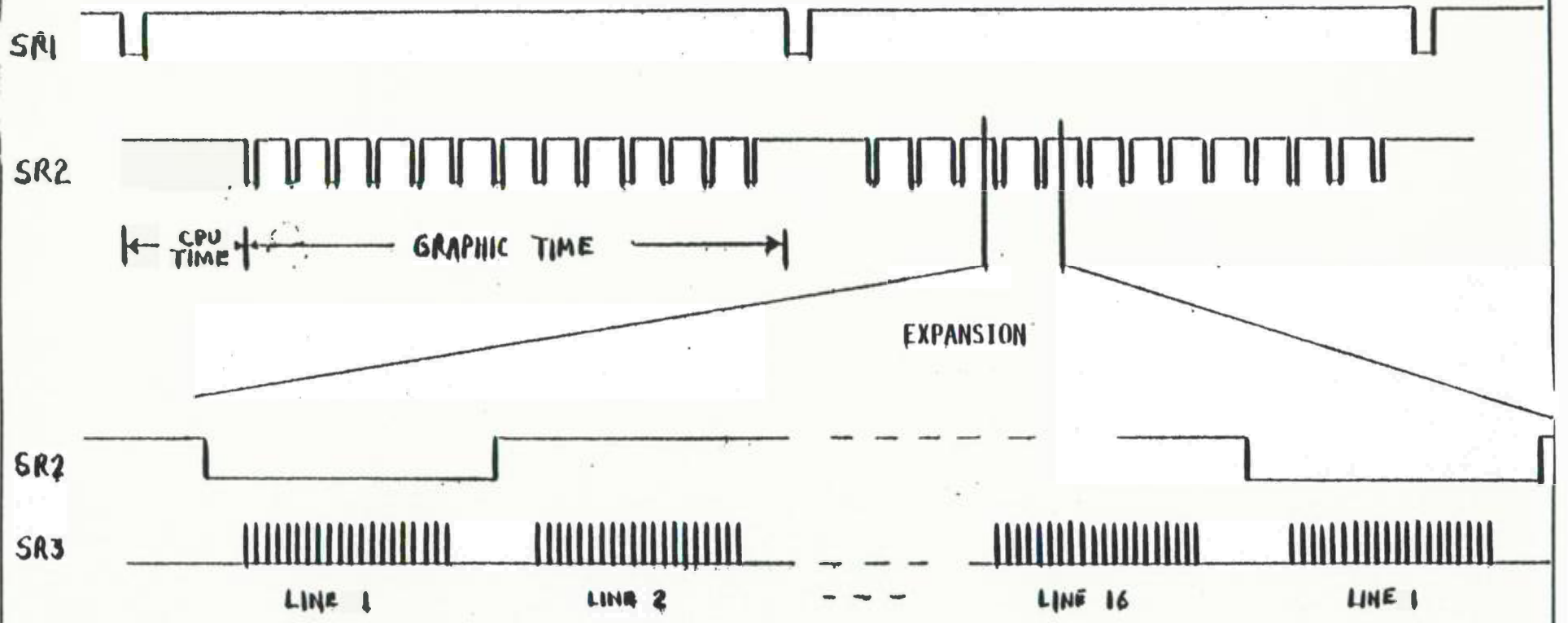


CPU TIME WRITE



STIC TIME READS

SYSTEM SYNCHRONIZATION TIMING

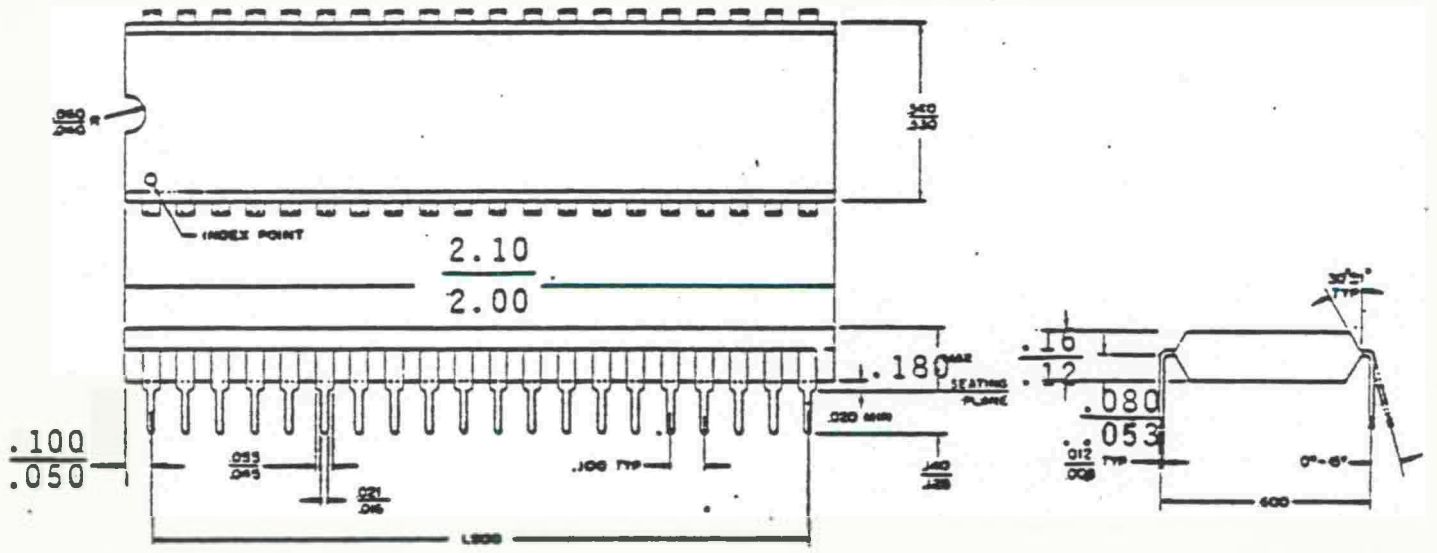


10.0 PIN CONNECTIONS

1	Vss	21	V2
2	SR3	22	V1
3	DWS'	23	SD13
4	DTB'	24	SD12
5	BAR'	25	SD11
6	BC2	26	SD10
7	BC1	27	SD9
8	BDIR	28	SD8
9	SR1	29	SD7
10	Ø1	30	SD6
11	Ø2	31	SDS
12	SR2	32	SD4
13	$\overline{\text{MSYNC}}$	33	SD3
14	RSTIN	34	SD2
15	Clock	35	SD1
16	V4	36	SDO
17	Vss	37	YO
18	V3	38	Y1
19	V5	39	Y2
20	Vcc	40	Vbb

11.0 MECHANICAL CHARACTERISTICS

11.1 PACKAGE DIMENSIONS



11.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

SPEC. NO.

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
F	5/7/82	13103		REWRITTEN			

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SHEET	1	2	3	4	5	6	7						
LAST REV	F	F	F	F	F	F	F						

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT — MICROELECTRONICS GROUP

TITLE: CUSTOMER PROCUREMENT SPECIFICATION
RO-3-9504-1XX, 2XX, 021

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED						SHEET 1 OF 7	
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	SPEC. NO.	REV
DATE	4/29/82	4/29	5/11/82	5/5/82	[illegible]		4.29.82	CPS-10040	F

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the AY-3-9504 N-Channel MOS, I.C. The patterns programmed into these cartridge ROMs are designated 1XX and 2XX for cartridge use and designated 021 for upper EXEC uses.

2.0 CIRCUIT FEATURES

- o Mask programmable storage providing 2048 X 10 bit words.
- o Memory map circuitry to place the 2K ROM page within a 65K memory area.
- o 10 bit tri-state bus with higher 6 bits driven to zero during read operations.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

5.0 CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1600 series microprocessor. It is configured as 2048 X 10 bit words and contains several features which reduce the device count in a practical microprocessor application. Two RO-3-9504 ROMS (1XX and 2XX patterns) make up one game ROM set and one RO-3-9504 ROM (021) is used as the upper EXEC.

6.0 OPERATING DESCRIPTION

From initialization, the 9504 waits for the first address code, e.g., BAR. For this address code and all subsequent address sequences, the 9504 reads the 16 bit external bus and latches the value into its address register.

The 9504 contains a programmable memory map location for its own 2K page, and if a valid address is detected, the particular address located will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus.

6.1 INPUT CONTROL SIGNALS

BD1R	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	-
0	1	0	ADAR	ADAR
0	1	1	DTB (READ)	DTB
1	0	0	BAR	BAR
1	0	1	DWS	-
1	1	0	DW	-
1	1	1	INTAK	BAR

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vss	-0.2V to +9.0V
Vcc with respect to Vss	-0.2V to +9.0V

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL SPECIFICATION

Ambient Temperature 0°C to +55°C

D.C. CHARACTERISTICS

Vss = 0.0V, Vcc = +4.85 to +5.15V

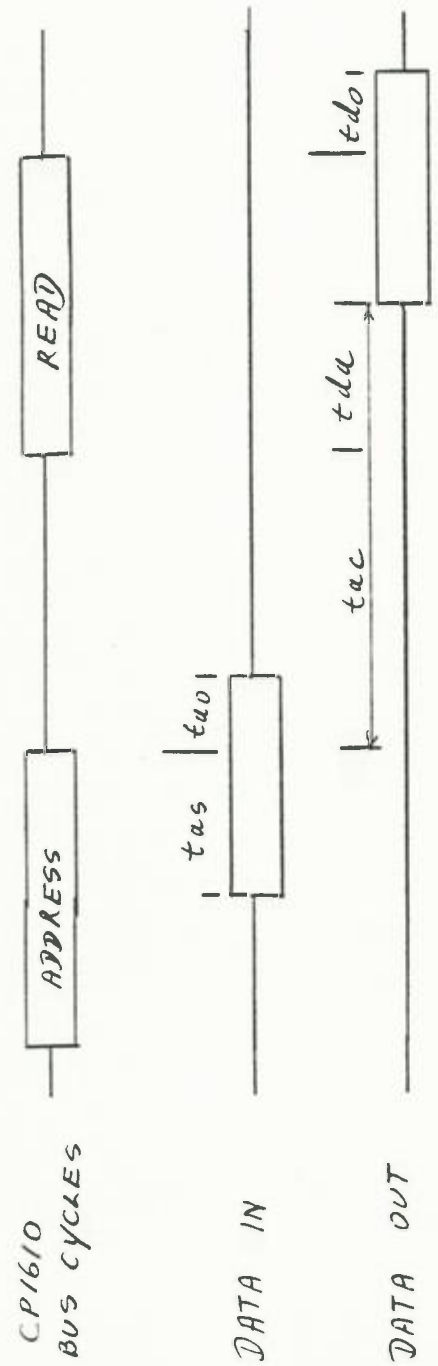
CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Bus and Control Inputs					
Input Logic Low	VIL	0	0.7	Volts	
Input Logic High	VIH	2.4	Vcc	Volts	
Leakage	IIL		5	ua	VIN = 0V to Vcc
CPU Bus Outputs					
Output Logic Low	VOL	0	0.5	Volts	IOL = 1.5mA]
Output Logic High	VOH	2.4	Vcc		IOH = 80uA] +150pf
Supply Current					
Vcc Supply	Icc		74	mA	at +55°C

A.C. CHARACTERISTICS

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address Set Up	tas	300		nSec	
Address Overlap	tao		65	nSec	
CPU Bus Ouputs					
Turn On Delay	tda		350	nSec	
Turn Off Delay	tdo	80	350	nSec	
Access Time	tac		1.5	uSec	

Note: Input capacitance of all logic pins, 10pf max VIN=0V @ 1MHz
Not measured during production test.

MEMORY TIMING

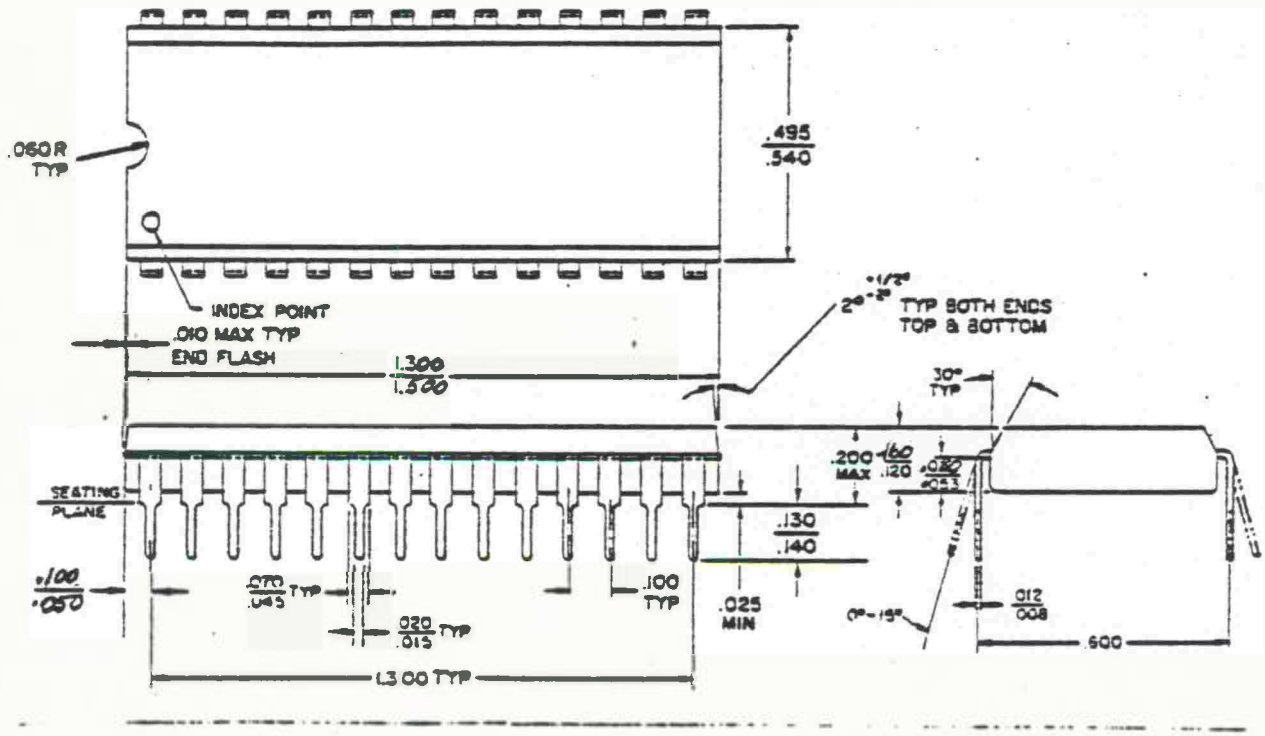


8.0 PIN CONNECTIONS

1	VCC	15	Vss
2	No Connection	16	DB7
3	No Connection	17	DB6
4	DB15	18	No Connection
5	No Connection	19	DB5
6	DB14	20	DB4
7	DB13	21	DB3
8	DB12	22	No Connection
9	DB11	23	DB2
10	OB10	24	DB1
11	No Connection	25	DB0
12	DB9	26	BDIR
13	OB8	27	BC2
14	No Connection	28	BC1

9.0 MECHANICAL CHARACTERISTICS

9.1 PACKAGE DIMENSIONS



9.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

REV	SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
SPEC. NO.					Company Confidential			
	H	5/7/82	13103		REWRITTEN			

GI DRAWING
AND SPEC. CONTROL
VALID COPY

SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13
LAST REV	H	H	H	H	H	H	H	H	H	H	H	H	H

SHEET	14	15	16	17	18	19	20	21 22	23 24	25 26	27 28		
LAST REV	H	H	H	H	H	H	H	H H	H H	H H	H H		

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT — MICROELECTRONICS GROUP

TITLE: CUSTOMER PROCUREMENT SPEC. AY-3-8900

PLANT

MODULE

OPERATION

	WRITTEN	APPROVED						SHEET 1 OF 28	
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	SPEC. NO.	REV
DATE	4/29/82	4/29	5/1/82	5/5/82	5-7		4/29/82	CPS-10042	H

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the functional description for the AY-3-8900 STIC MOS I.C.

2.0 CIRCUIT FEATURES

- o Outputs include coded signal timings for CCIR video signal generation.
- o Operation from a 4.0000 MHZ clock.
- o 8 coordinate addressable foreground objects on a grid of 167H by 105V of which 159 x 96 are visible positions.
- o Foreground objects independently programmable for half height, y zoom, x zoom and 8 or 16 character lines high.
- o Selectable background display on a matrix of 20 H by 12 V using 8 x 8 picture elements.
- o 16 digitally selectable colors.
- o Capable of accepting data, address and graphics information on common multiplexed bus.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit will be subjected to the electrical parameters given in the CPS.

4.1 FUNCTIONAL TESTING

The AY-3-8900 must be functional in a Use Test defined in CPS-10049.

4.2 TARGET FAILURE RATE (at 25°C)

The post burn-in (40°C, 6 hours operational) target failure rate for this device is 0.85 percent per thousand hours (average target failure rate). This number is based on an exponential failure distribution and a thermal activation energy of 1.0ev.

5.0 SYSTEM DESCRIPTION

The AY-3-8900 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility, which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900 operates within the computer system by time sharing a bi-directional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900 has switched to the CPU controlled mode.

SR2 is issued thirteen or fourteen times per picture frame. The AY-3-8900 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also used during the CPU controlled mode to operate as a drive selector on the 14 bit bus.

The second control bus is used to specify address, read and write sequences on the area of external memory used to store the graphic character "dot" patterns. The three signals on this bus are BAR', DTB' and DWS'. The BAR' is output by the AY-3-8900 when a valid graphics character address is on the 14 bit bus. The external memory must latch this address for future read or write operations. The DTB' signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit bus. The DWS' signal indicates that a "write" is requested and the external memory must complete the sequence within 625 nanoseconds.

5.0 cont.

The graphic control bus is used during "STIC" time in the fetch of "foreground" object patterns and "background" object patterns. During the non-"STIC" time when the CPU is in command, the graphics control bus is used in a semi-copy mode to link the memory area containing the graphic patterns into the main memory area of the external microprocessor.

The third control bus communicates with the external CPU. This bus comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control but is only validated if the AY-3-8900 is in the CPU controlled mode, otherwise it is ignored.

6.0 DATA STRUCTURES

6.1 HORIZONTAL POSITION DATA WORD

8 bits of an 11 bit word are used to control the horizontal positioning of a foreground object to a visible resolution of one part in 167.

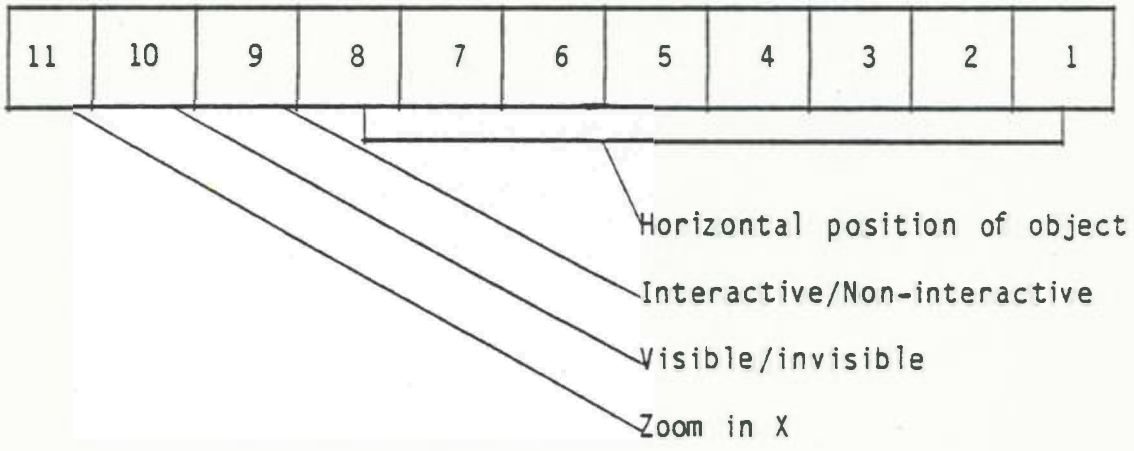
The actual X coordinate positions are 8 to 167 and the extra seven locations are used to permit objects to progressively "disappear" into the border area.

The extra seven locations are on the left hand side and effectively give a negative positioning of seven units off the screen. Any object would disappear if moved to the right since the X coordinate is the left hand edge of the character.

The data for the objects are loaded into address locations $(0)_8$ through $(7)_8$ in STIC. The lower eight bits of the word (DB0-DB7) defines its horizontal position. The ninth bit selects whether the moving object is interactive or non-interactive. The tenth bit controls the visability, and using this bit in conjunction with the interactive bit, all combinations are possible.

The eleventh bit is an X zoom control which, if set to a logic 1, clocks out the object shift register at half speed which doubles the object size displayed on the screen in the X direction.

The horizontal position bits are designated as follows:



6.2 VERTICAL POSITION DATA WORD

7 bits of a 12 bit word are used to control the vertical positioning of each moving object to a resolution of one part in 104.

The actual Y coordinate positions also allow objects to disappear top or bottom and an extra eight positions are provided above the top of the active screen area.

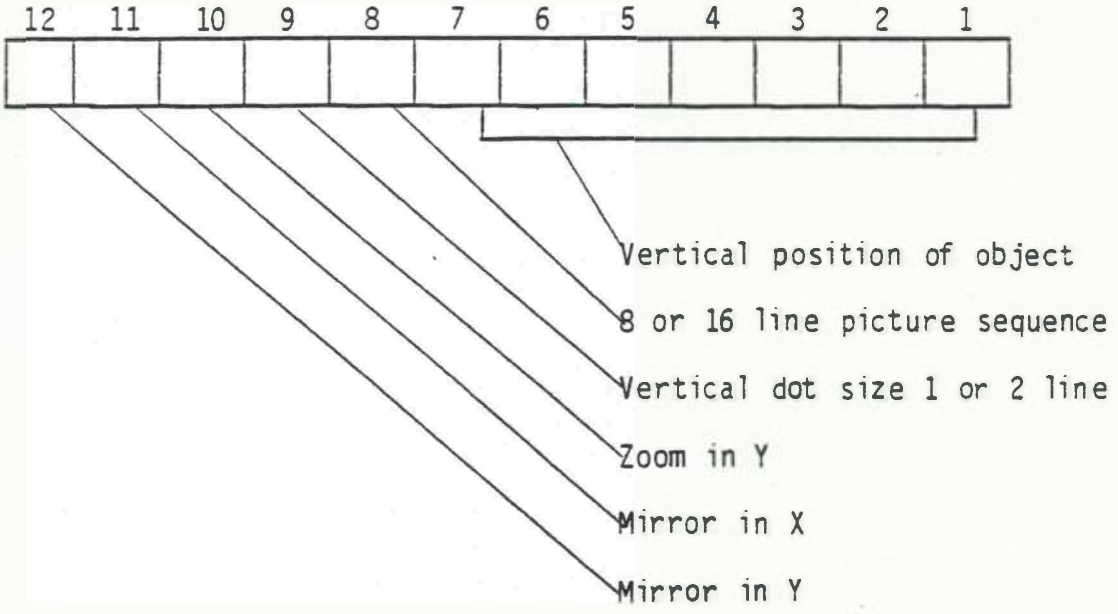
The data for the Y coordinate positions are loaded into address locations $(10)_8$ through $(17)_8$ within STIC. The lower seven bits of the word define the vertical Y position of the top edge of the object. The eighth bit allows the character to be drawn as an 8 X 8 matrix or an 8 X 16 matrix. The significance of the larger matrix is that you can have a higher resolution object by using the half height feature or it may simply be used to draw more complex shapes within the vertical rectangle. If a sixteen line picture (data changes) is required, the start position for the character address in memory must have the lower bit (DB3) at a logic zero to allow STIC to consecutively address sixteen eight-bit words. The data patterns within the memory must be organized to allow sixteen line characters to occupy two consecutive eight byte blocks within the graphics memory area. (STIC provides the lower four bit binary, current line address to memory rather than a three bit code as used in eight line pictures).

The ninth bit controls ther vertical size of the minimum picture element PIXEL. Throughout the description of AY-3-8900 character display capabilities, the minimum picture element, PIXEL, is defined as a "square" having a timed width equal to the period of the reference crystal, approximately 250 nSec., and a vertical height of two drawn lines on a non-interlaced 312 line half frame. The "foreground" or "moving" objects have a half height control which allows a pattern change on all drawn lines instead of every second line, and this reduces the minimum PIXEL to 250 nSec by one drawn line. The ninth bit control, if set to a logic 1, causes the corresponding moving object to be drawn over eight video lines instead of the normal sixteen lines.

6.2 cont.

The eleventh and twelfth bits respectively control the X and Y mirror. The tenth bit controls Y zoom and operates in a binary manner with the 1 or 2 line select bit to provide a vertical selection of 1, 2, 4, or 8 drawn lines before a data change. The maximum height object would be sixteen data lines times 8 which is 128 visible lines.

The vertical position bits are designated as follows:



BIT 10	BIT 9	
0	0	Data change each line
0	1	Data change every two lines
1	0	Data change every four lines
1	1	Data change every eight lines

6.3 FOREGROUND OBJECT IDENTIFICATION AND CONTROL

Locations $(20)_8$ through $(27)_8$ within STIC store the object library address bits and the color and control information for the eight foreground objects. The lower three bits select a 1 of the first 8 available colors. The next 9 bits are the character start address from a library of 512 possible characters. The thirteenth bit operates in conjunction with the three color bits to give a 1 from 16 color selection. The fourteenth bit controls the display priority of that particular foreground object relative to the background. A logic zero in this bit allows the foreground object color to replace any background character where there is an overlap of the drawn image. The foreground objects themselves have a related priority in that a lower numerical object has a higher visible priority that a higher numerical object, i.e, object zero takes precedence over all other objects, object one covers all except zero, etc. The priority draw is conditional upon the object being visible. If an invisible object has been programmed it can be interactive with all other objects but it will not enter the priority draw logic. This stops invisible foreground objects from producing a 'negative' effect if it has a priority over any background character which it may overlap.

The effect of priority defines who should control the color display on areas which overlap. Because the priority may be changed on any half frame, this may be used by the programmer to produce a three dimensional effect of objects being in front of some background displays and behind others. The identification and control words are designated as follows:

14	13	12	11	10	9	8	7	6	5	4	3	2	1
MK1	MK2	CHARACTER START ADDRESS									C2	C1	C0

BIT	FUNCTION	LOGIC 0	LOGIC 1
MK1	Priority Control	Foreground	Background
MK2	Color Control	Group A	Group A and B

6.4 FOREGROUND OBJECT COMPUTER CONTROL

The CPU must accept the 8900 STIC with a memory map of 0_8 to 77_8. In general most words or bits are read/write but there are some exceptions. The bit controlling the CPU release of the 14 bit bus called 'Special Bit', is write only to the CPU. The interaction words at $(30)_8$ to $(37)_8$ are set by the STIC and can set or be reset by the CPU.

There are three words controlling each of the eight foreground objects, an X coordinate, a Y coordinate and an object descriptor.

6.5 FOREGROUND OBJECT INTERACTION

Moving Objects - During display of the active picture, all interactive objects are optionally inspected for overlap with other interactive objects. An "overlap" is defined such that a logic 1 or active area of one object is overlapped on a logic 1 of any other object. Either or both objects may be invisible.

If an overlap is detected, the hit signal is stored in an eight word array positioned at addresses $(30)_8$ to $(37)_8$ within STIC. The array is organized as eight by ten bit words and the lower byte is assigned a matrix with significance relative to the numerical value of the object. Word zero, bit zero is used for object zero, bit one for object zero overlapping with object one, etc. The bit apparently available for an object interacting with itself are wired to a permanent zero and cannot be set by the CPU.

	BR	BD	7	6	5	4	3	2	1	0
Object 0	0	0	0	0	1	0	0	0	1	0
1	0	1	0	0	0	0	1	0	0	1
2	1	0	0	0	1	0	0	0	0	0
3	0	0	0	0	0	0	0	0	1	0
4	0	1	0	1	1	0	0	0	0	0
5	0	0	1	0	0	1	0	1	0	1
6	0	0	0	0	0	1	0	0	0	0
7	0	0	0	0	1	0	0	0	0	0

BD - Background Character

BR - Border

Above is a possible pattern within the interaction matrix.

Background Objects - bit nine of the interaction matrix is used to indicate if a foreground object overlapped any background object. A background object is defined as a character pattern drawn in the background mode or any color which is not white if drawn in the colored squares mode.

Border - The eight foreground objects are inspected against a border "window", and if an interactive character is overlapping the edge of this "window" the tenth bit of the Interaction Word will be set to a logic one.

6.6 COMPUTER CONTROL OF INTERACTIONS

The interaction record area of STIC is set by any shape overlap if the appropriate interaction bit has been set. The STIC gives control to the CPU from the start of an interrupt period by issuing SR1. At this time the CPU can inspect interactions and perform the normal timed object movement. The STIC is not completely disabled at this time and it still allows the CPU to pass data to and from the graphics memory area using STIC logic for timing and control signals. There is a location within STIC at address 40_8 which is the CPU-STIC control known as Special Bit. This location may be reset to a logic zero by writing from the CPU, and this must occur during the next 6.4 mSec, if the next half frame is to be drawn by STIC. If the interaction matrix has not been cleared prior to the STIC being allowed to display a new half frame, any new interactions will OR with the old data.

6.7 BACKGROUND OBJECTS

The background display of the 8900 STIC system is organized into a matrix of twenty horizontal positions by twelve vertical positions for a total of 240 locations. The 240 selection words are accessed in sequence from external memory.

Each "card" location on the screen is defined completely by a 14 bit word. The three least significant bits defined the 1 of 8 colors of the object to be displayed and is used on conjunction with control bit BK2 (DB12) to product a choice of 1 of 16 colors. The next nine bits define the character start address from an external library of 512 characters. The individual rows within a character are read automatically by the B900 using a Y0, Y1, Y2 three line connection.

The top three bits of the word (DB11, DB12, DB13) are control bits which describe some extra features available during the background display. There are three modes under which these codes can be interpreted. Two of these operate on the background color wash and the third code specifies the colored squares mode. These modes are explained in greater detail under a separate heading.

The drawing sequence for background characters is defined by timing logic within the 8900 and control logic within the system RAM. The system is synchronized by the SR1 (interrupt) signal from the STIC, which is a negative going edge generated one line after the end of active picture.

6.7 cont.

The CPU accepts this signal as an interrupt request and in sequence it will issue an acknowledge, INTAK, on the control bus, BC1, BC2, BDIR. The INTAK is decoded by the STIC and used to clock SR1 back to a logic one condition.

The timing of the background data fetching it synchronized with SR2 and SR3. The first SR2 signals the start of STIC time to the 9600. Subsequent SR2s indicate that a new row of characters has been requested by the 8900. SR3 is pulsed positive to request each individual character descriptor.

6.8 BACKGROUND MOTION

The entire background field may be moved by programming horizontal and vertical offset words which are located at address 60_8 for X and 61_8 for Y. These words are of three bits and they are used to provide an offset of the picture origin by an amount of up to eight counts in X and Y at the full resolution of the system.

The non-offset condition is 0, 0 in the two stores and as the numbers are increased, the "picture" origin will correspondingly move right and down. To remove the effect of a "wrap around" display where half an object is at the top and half at the bottom, or left and right as the case may be. There are two control bits at address 62_8 where bit zero can be set to a one to effectively extend the left hand border to cover the first column of cards. Bit one is used to extend the top border to cover the first row. For all conditions other than 0, 0 in the offset words, there will still be a 20 X 12 card display with fractional cards around the periphery. The X and Y offset and their control bits are completely independent and may be used in any combination.

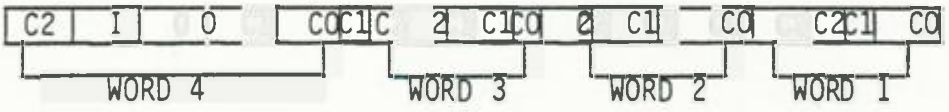
Note that the origin for the background display and the foreground positions are locked together and that a moving background will also move the foreground.

6.9 COLORED SQUARES MODE

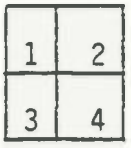
To extend the universal application of the 8900, an extra capability is provided for more color programmability than the basic one object on one card approach.

This extra mode is colored squares and it operates by taking an individual 8 X 8 card and redefining it as four 4 X 4 squares. Each of the 4 X 4 squares can be programmed separately to one of eight colors (from Group A). If all the background matrix was selected in colored squares mode, this would provide an array of 40 X 24 where each of the 960 squares are separately programmed for color.

The colored square word is designated as follows:



The three color bits of each of the four words directly defines the color inside the corresponding square. The condition of three ones which would be a white square, is trapped by the display logic and the current background color is drawn from that square.



7.0 BACKGROUND COLOR

There are two modes available which provide control of the background color wash. The particular mode selected is defined by the CPU writing or reading address 41_8 within the 8900. The background color wash mode must remain stable throughout any particular frame of 240 cards but may be changed during the CPU interrupt time initiated by SR1.

Mode 1 - If address 41_8 is read by the CPU, the 8900 will operate in the first background mode. This mode uses a four word, four bit cyclic stack and a stack pointer. The four words are positioned at 50_8 - 53_8 on DB0 - DB3 inclusive, and may be accessed by the CPU during the interrupt period following SR1. The stack pointer is controlled by BK1 and a logic zero will leave the pointer at its current position, a logic one will step the pointer to the next position. The stack is a continuous loop and will carry around the end position. When the pointer is incremented the new color wash will appear on the card which caused the increment.

7.0 cont.

The use of the colored squared code in any "card" position inhibits the action of BK1 and redefines it as the C2 control bit, thereby holding the stack pointer at its current position.

The pointer is reset to the top of the stack at the end of active picture.

Mode 2 - If address 41_8 is written to by the CPU, the 8900 will operate in the second background mode. The 14 bit word is now coded to contain program information for both the background character color and the color wash behind that character. This allows the programmer to define a colored "object" on a colored checkerboard effect with complete control of any random color changes necessary.

The recording of the background descriptor to add the background color wash reduces the character address word to six bits, allowing two further bits for use in color coding. The three bits of background control, BK1, BK2, and BK3 are also redefined.

7.0 cont.

BACKGROUND MODES:

MODE 1:

	BK1	BK2	9 BIT CHARACTER ADDRESS	C2	C1	C0

BK1	BK2	BK3	BACKGROUND COLOR
0	0	X	Group A - Current
1	0	X	Group A - Next
0	1	X	Group B - Current
1	1	X	Group B - Next
X	1	0	
X	1	0	COLORED SQUARES
DB13	DB12	DB11	

COLORED STACK

COLOR STACK POINTER

A/B	C2	C1	C0
A/B	C2	C1	C0
A/B	C2	C1	C0
A/B	C2	C1	C0

MODE 2:

C2	BK2	BK3	C1	C0	6 BIT CHARACTER ADDRESS	C2	C1	C0

C2, C1, C0 - color code for background wash

BK2 - A/B control bit, operates on color wash and not on character color for mode two.

A logic zero selects first option, logic one selects second.

7.1 BORDER COLOR

The active area of the display is surrounded by a colored border. The border may be drawn in any of the sixteen colors, and it may be programmed by the CPU via a four bit store at address 54_8, which is adjacent to the background color storage. The border color is programmed during the interrupt period following SR1 and it may be changed in any half frame.

8.0 STIC TIMING

The basic timing of the device can be segregated into three operating areas. These areas are directly related to the real time raster scan operation of a domestic television receiver.

The areas are:

1. Active drawn line
2. Active line retrace
3. Vertical retrace period

1. The Active Drawn Line defines the period when a row of selectable dots are being drawn on the television screen. During this time a single video line from a row of "background" characters is drawn, using the control signals SR2, SR3, BAR', DTB' in combination from an area of external memory.

   The visible dot patterns for a "foreground" object are also output at this time.

2. The Active Line Retrace is the period when the dot pattern for the individual "foreground objects are fetched from external memory. The control signals which are active at this time are BAR' and DTB'.

3. The Vertical Retrace Period extends from the last line at the bottom of the active picture until a period two lines before the restart of the active picture. The AY-3-8900 indicates the start of the retrace operation by issuing a negative pulse on SR1. This pulse is used by the external CPU as an indication that the STIC internal memory has finished accessing. The end of the vertical retrace period is signified by a negative pulse on SR2. At this point, the CPU will lose access to the memory area contained within the 8900 chip, if special bit has been set. To allow the CPU to access memory on the 14 bit bus the 8900 chip operates so that the three lines SD0, SO1, SD2 and Y0, Y1 and Y2 can copy bi-directional under control of the CPU bus BC1, BC2, BDIR.

9.0 ELECRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vbb	-0.2V to +9.0V
Vcc, Vdd & Vss with respect to Vbb	-0.2V to +9.0V

*NOTE:

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For definition of control signal codes on BC1, BC2, BDIR, please refer to sheet 3 CPS-10036.

OPERATIONAL SPECIFICATION

Ambient Temperature 0°C to +55°C

D.C. CHARACTERISTICS

Vss = 0.0V, Vcc = 5.45V to 5.95V, Vbb = -2.1V to -2.4V

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Bus Inputs					
SD0-SD13, Y0-Y3					
Logic Low	VIL		0.7	Volts	
Logic High	VIH	2.4		Volts	
Leakage	IIL		5	uA	VIN = 0V to Vcc
Bus Outputs					
SD0-SD12, Y0-Y3					
Logic Low	VOL	0	0.5	Volts	IOL = 100uA] +100pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
Control Inputs					
BC1, BC2, BDIR, RSTIN, CLOCK					
Logic Low	VIL		0.7	Volts	
Logic High	VIL	2.4		Volts	
Leakage	IIL		5	uA	VIN= 0V to Vcc
Control Outputs					
SR1, SR2, $\overline{\text{MSYNC}}$					
Logic Low	VOL		0.5	Volts	IOL = 500uA] +100pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
BAR1, DTB1, DWS1					
Logic Low	VOL		0.5	Volts	IOL = 100uA] +50pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
SR3					
Logic Low	VOL		0.5	Volts	IOL = 100uA] +50pf
Logic High	VOH	3.0	Vcc	Volts	IOH = 100uA]

D.C. CHARACTERISTICS (cont.)

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Outputs					
Ø1, Ø2					
Logic Low	VOL		0.5	Volts	IOL = 1mA] +100 pf
Logic High	VOH	2.4	Vcc	Volts	IOH = 100uA]
Power Supply Current					
Vcc	Icc		170	mA	at +55°C
Vbb	Ibb		3	mA	

Note: Input capacitance of all logic pins, 10pf max
VIN = 0V @ 1MHz.
Not measured during production test.

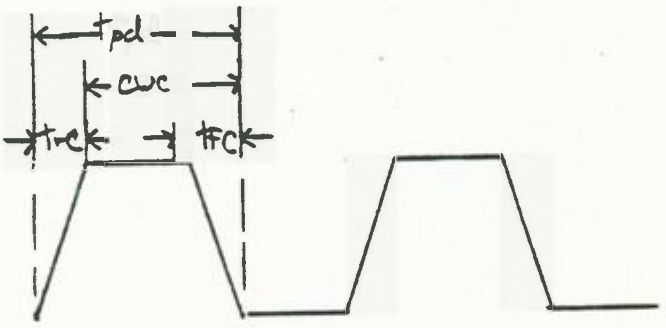
A.C. CHARACTERISTICS

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Clock Input Freq.	fc	-	-	MHz	4.000000 externally
Rise Time	trc		30	nSec	adjusted
Fall Time	tfc		20	nSec	
Pulse Width	cwc	100	130	nSec	
CPU Time					
Data Bus (input) SD0-SD13					
Address Set Up	tas	150		nSec	
Address Overlap	tao	30		nSec	
Write Set Up	tws	400		nSec	
Write Overlap	two	200		nSec	
SD0-SD2 to Y0-Y2 bus copy	tdy		125	nSec	Data valid at start of copy
Data Bus (output) SD0-SD13					
Turn On Delay	tda*				
Turn Off Delay	tdo*				
Y0-Y2 to SD0-SD2 bus copy	tyd		200	nSec	Data valid at start of copy
BC1, BC2, BDIR Setup	tcs	0		nSec	
BC1, BC2, BDIR Overlap	tco	250		nSec	

*For a BAR or ADAR within the STIC or GRAPHICS memory address the STIC will perform a look-ahead READ immediately after the valid address. The following DTB signal is only used to disable the READ sequence at the appropriate time. If a WRITE sequence is detected the look-ahead READ is disabled in DW time and a valid WRITE procedure is completed during DWS.

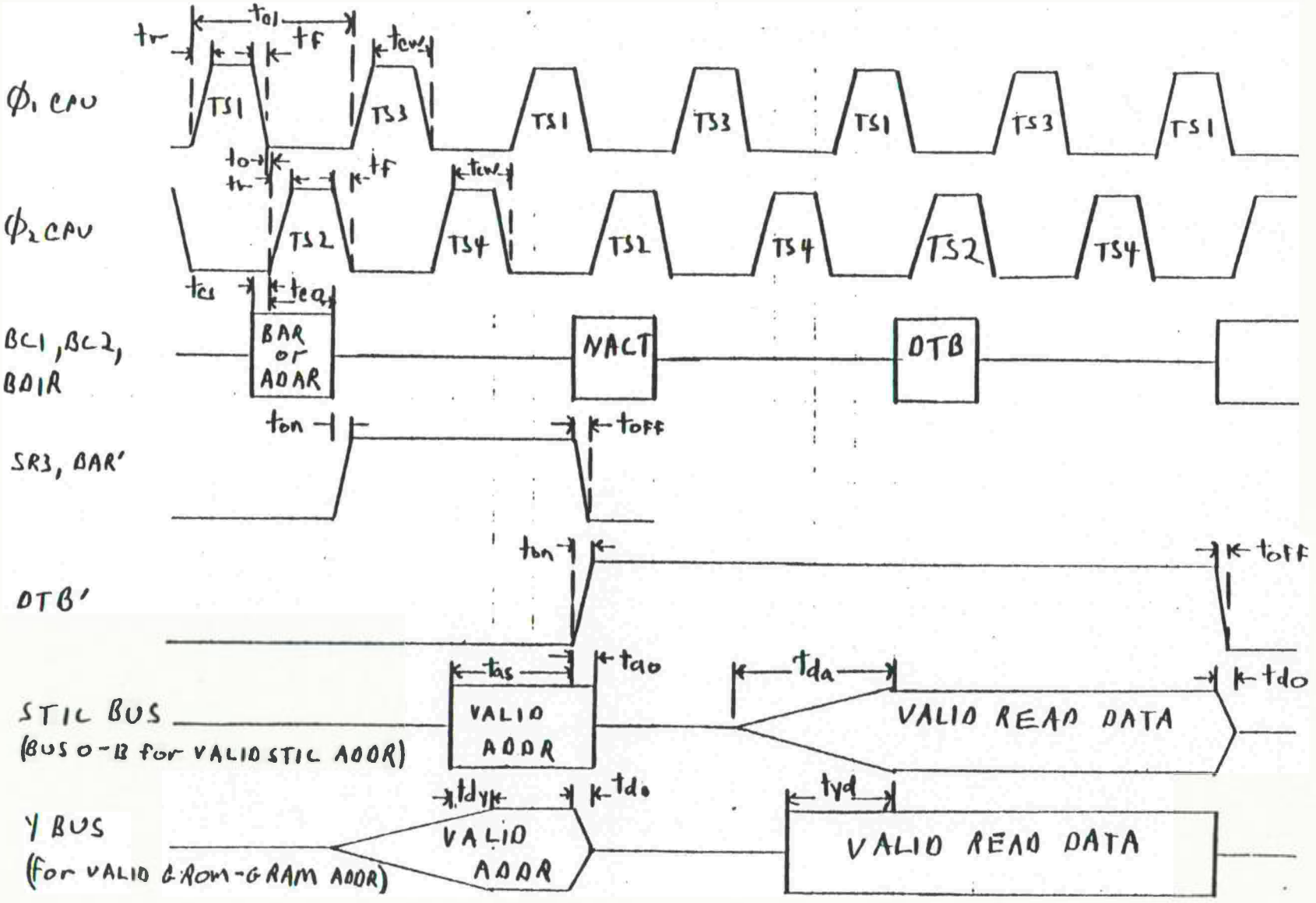
Clock Outputs Ø1, Ø2					
Rise Time	tr		40	nSec	
Fall Time	tf		30	nSec	
Overlap	to	0		nSec	
Pulse Width	tcw	170		nSec	
Control Turn On SR3, BAR[1], DTB[1] DWS[1]	ton		40	nSec	
Turn Off	toff		40	nSec	

STIC TIME	MIN	MAX	UNITS
Background Period			
Control Signals			
SR3 Turn On 0		40	nSec
SR3 Turn Off 0		40	nSec
BAR^1, DTB^1, Turn On 0		40	nSec
BAR^1, DTB^1, Turn Off 0		40	nSec
Y Bus Drive Ø↓		250	nSec
Graphics Bus Read			
Set Up DTB^1 ↓		200	nSec
Hold DTB^1 ↓	0		nSec
Foreground Period			
SB and Y Bus Drive Ø↓		250	nSec
SB and Y Bus Hold Ø ↓	0		nSec
Graphics Bus Read			
Set Up DTB^1 ↓		200	nSec
Hold DTB^1 ↓	0		nSec

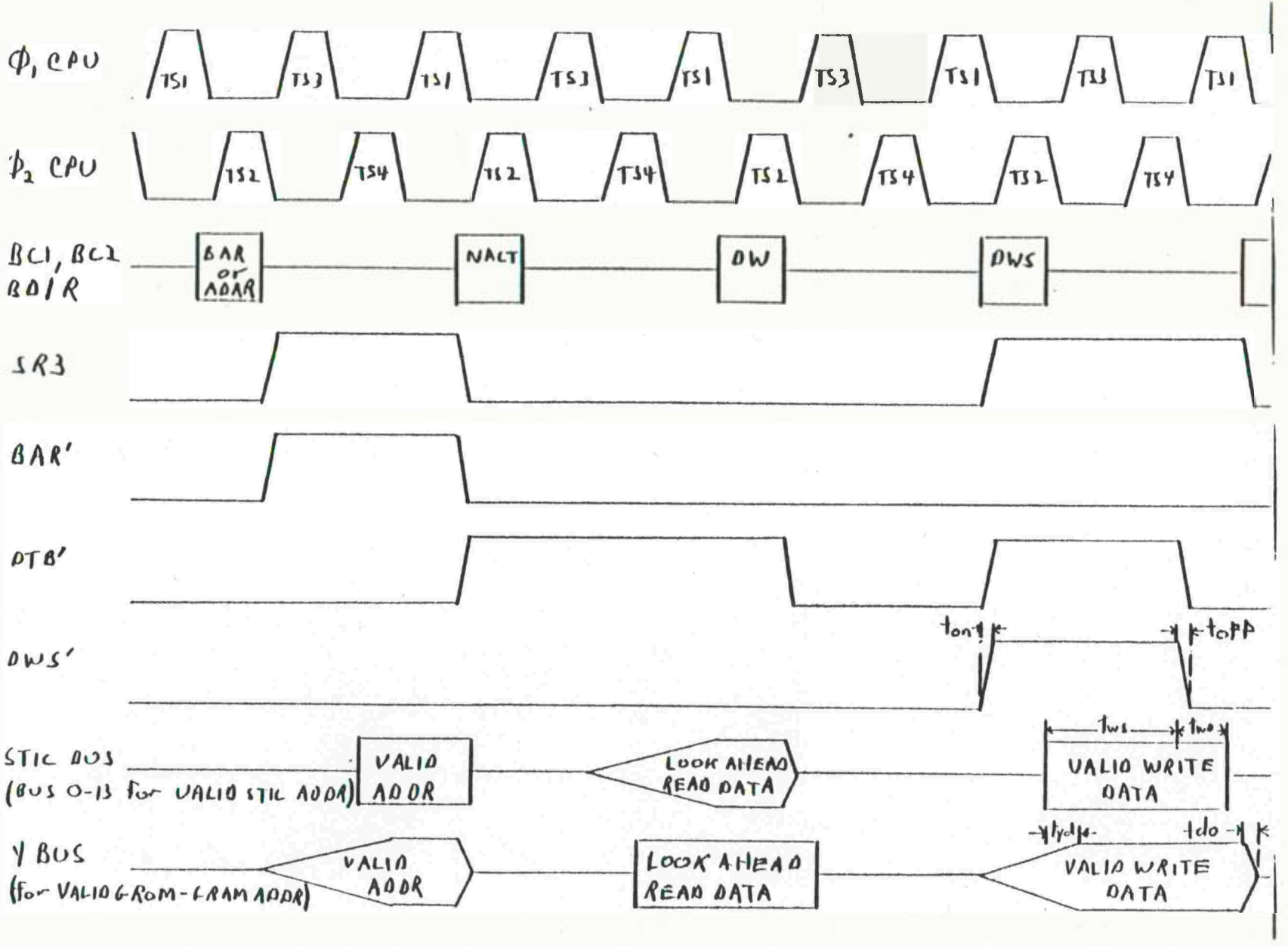


STIC INPUT

CLOCK



CPU TIME READ



CPU TIME WRITE

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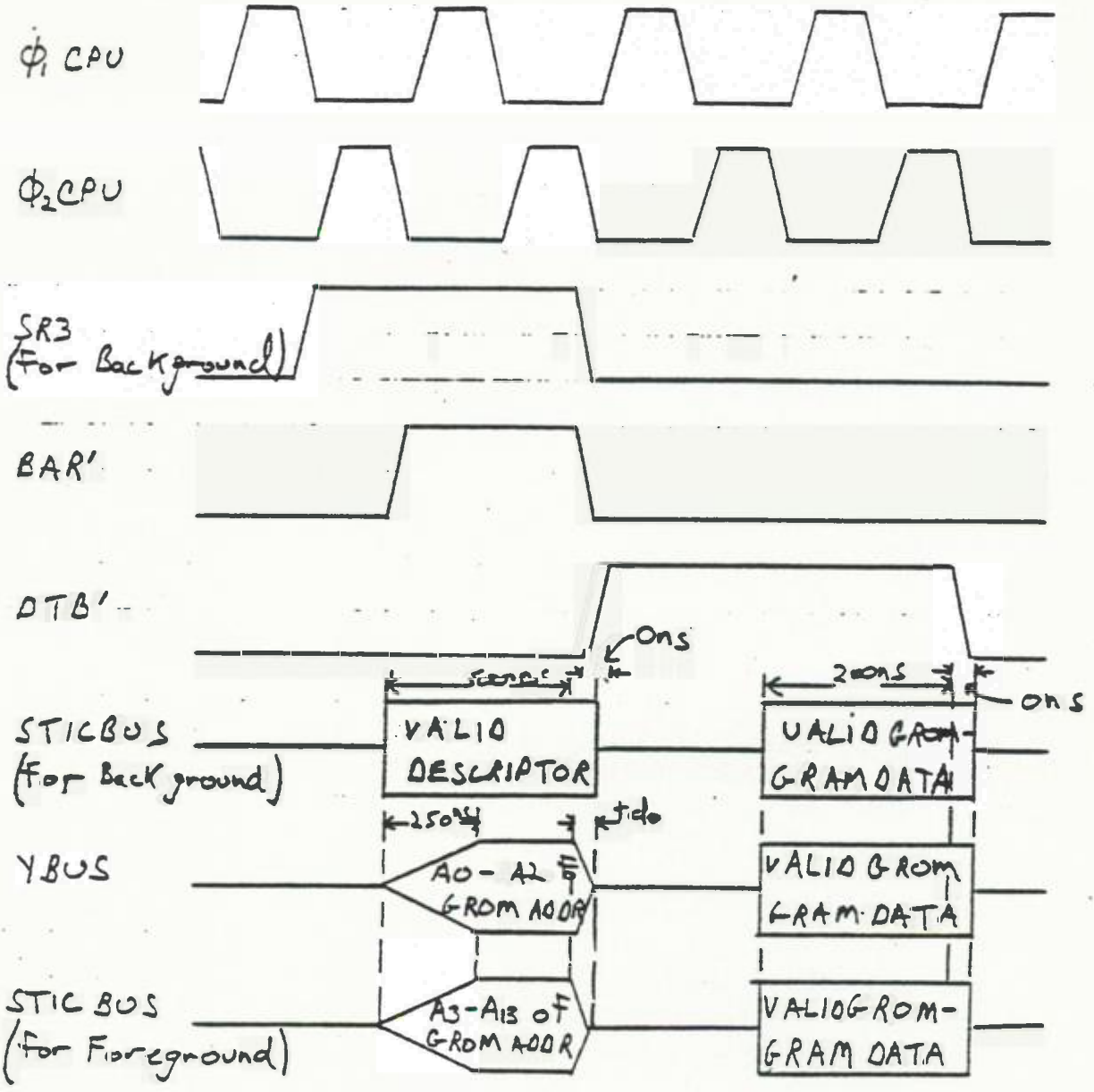
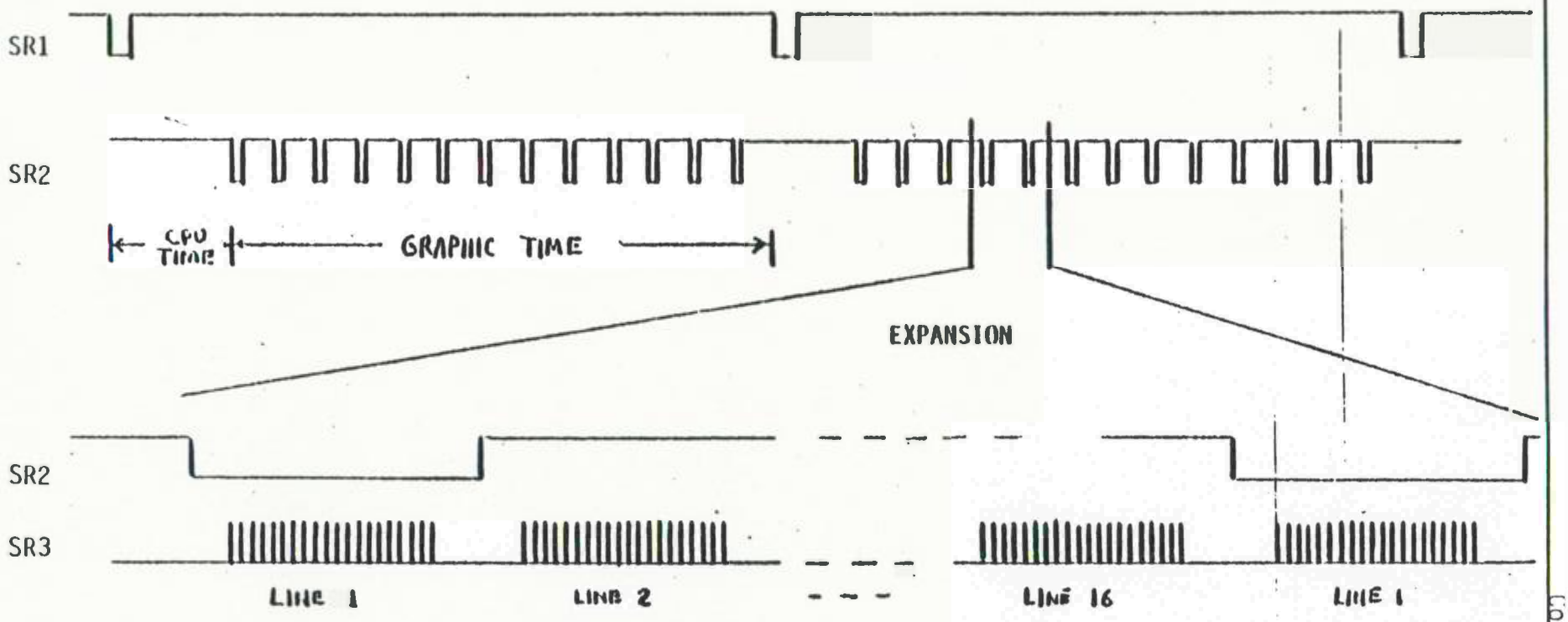


STIC TIME READS

SYSTEM SYNCHRONIZATION TIMING



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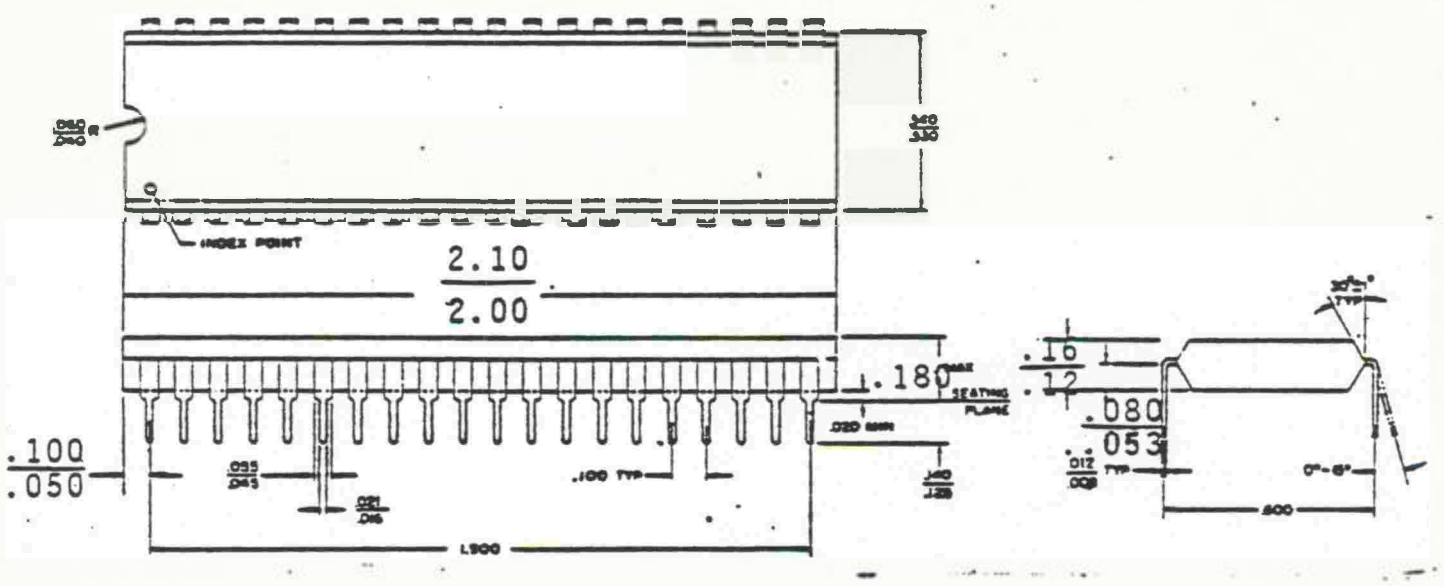
10.0 PIN CONNECTIONS

1	Vss	21	C2
2	SR3	22	C1
3	DWS'	23	SD13
4	DTB	24	SD12
5	BAR	25	SD11
6	BC2	26	SD10
7	BC1	27	SD9
8	BDIR	28	SO8
9	SR1	29	SO7
10	Ø1	30	SO6
11	Ø2	31	SD5
12	SR2	32	SO4
13	$\overline{\text{MSYNC}}$	33	SO3
14	RSTIN	34	SO2
15	Clock	35	SD1
16	C5	36	SO0
17	Vss	37	YO
18	C4	38	Y1
19	C3	39	Y2
20	Vcc	40	Vbb

11.0 MECHANICAL CHARACTERISTICS

11.1 PACKAGE DIMENSIONS



11.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
D	5/7/82	13103		REWRITTEN			

SPEC. NO.

SHEET	1	2	3	4	5	6	7	8					
LAST REV	D	D	D	D	D	A	A	A					

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT — MICROELECTRONICS GROUP

PLANT

MODULE

OPERATION

TITLE CUSTOMER PROCUREMENT SPECIFICATION

MATTEL INTELLIVISION SYSTEM USE TEST

	WRITTEN	APPROVED					
BY	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
DATE	4/28/82	4/29	5/1/82	5/6/82	[illegible]	4/29/82	

SHEET 1 OF 8

SPEC. NO. CPS-10043

REV D

MATTEL INTELLIVISION SYSTEM USE TEST

This unit test has been devised to allow the Mattel Intellivision System to be self-tested using specially programmed test cartridges, (Board Number 39-121 Rev. E or equivalent) consisting of RO-3-9504-207. Individual kits of IC's are tested as complete systems on an Incoming Material Inspection (IMI) Station, which consists of Logic Board 39-133 Rev. X1 (or substitute mutually agreed upon by General Instrument and Mattel) with Z.I.F. lever sockets in place to test the various General Instrument supplied IC's. The test board also contains power supplies capable of switching over the range of V_{DD}, V_{CC}, V_{BB}.

The following test procedure is to be iterated over appropriate combinations of the supply voltages which are:

V_{DD} = 11.64 to 12.36V

V_{CC} = 4.85 to 5.15V

V_{BB} = -2.1 to -2.4V

V_{CC} for AY-3-8900-1 = V_{CC} + .7 $\pm$ .1V

After connecting the IMI test board to a color T.V. receiver and plugging in the 120V line, insert the self-test cartridge and turn the test board power switch on, switch to the RO-3-9504 003 IMI ROM pair.

Depress reset with no switches depressed on the left hand controller. This will immediately bypass the hand controller test and proceed to the automatic tests (Step 3).

In order to initially test the hand controllers, depress buttons 1 and 7 on the left hand controller and depress the reset switch. An individual test menu will appear. Depress the enter switch on the left controller.

1. Then observe the picture on the T.V. screen (Fig. 1). The test is to verify the color bars generated on the bottom of the screen. Each color should match the corresponding color given in Fig. 1. Missing colors or any serious variation of the picture may require a recalibration of the oscillator frequency Pin 15 for 3.579545MHz $\pm$10Hz. Adjustment may be obtained by the variable capacitor on Pin 2. After recheck of picture with correct frequency on Pin 15, the video should match Figure 1 or the AY-3-8915 is rejected. NOTE: The video signals generated by the AY-3-8915 are intended to be the video input of an R.F. modulator, for use on a T.V. receiver designed for the reception of N.T.S.C. transmission standards as adopted by the F.C.C. As a result of there being no absolute standards for color production, the colors as defined here are relative and subject to individual interpretation.

2. This part of the test is a manual check on the controller functions as inputs through the two I/O ports on the AY-3-8914 sound generator.

   a. Depress each number button on both controllers sequentially, then depress the buttons on the edge of each controller for fire and left and right controls. As the buttons are depressed, the appropriate numbers, plus fire, left and right indicators on the screen should turn from yellow to white to indicate verification. NOTE: The fire buttons are ganged in the controller and both F indicators will turn from yellow to white on the screen when either fire button is depressed.

   b. Depress and rotate the directional pad on each controller. An arrow will appear on the pad outline on the screen indicating corresponding position depressed. Both controllers should be tested in the same manner.

   c. Depress the numbers 1 and 9 simultaneously on either controller and the self-test will then proceed to the automatic testing.

3. The T.V. will show various patterns as the test runs by itself. Failures in the DUT may show up as various written failure statements on the screen, or the program may stop the timer indicator and/or blank out the entire picture.

4. After the automatic tests are through, a sound test is begun:

   a. A note starting at a high octave, stepping down through five octaves, three consecutive times. This checks each of the three analog outputs.

   b. A random noise (or hiss sound) starting at high frequency noise and decreasing to lower frequency noise. This tests the noise generator.

   c. A single-tone starting at maximum volume and decreasing in steps. This is a check on the amplitude control.

   d. Two gunshot sounds, one at full volume and one at half volume. This tests the envelope shape and cycle control.

5. Near the end of the self test the screen should display four lines of eight distinct colors with an overlapping stack of eight squares, each a distinct color also (See Fig. 2). The operator must make a visual check on the colors and shapes produced. Depression of the clear button accepts the display test. Depression of the enter button fails the display test.

6. The next test consists of watching for the words "MODE TWO" being alternately displayed with the colored squares pattern detailed in Fig. 3. Depression of the clear button accepts the test, depression of the enter button fails the test.

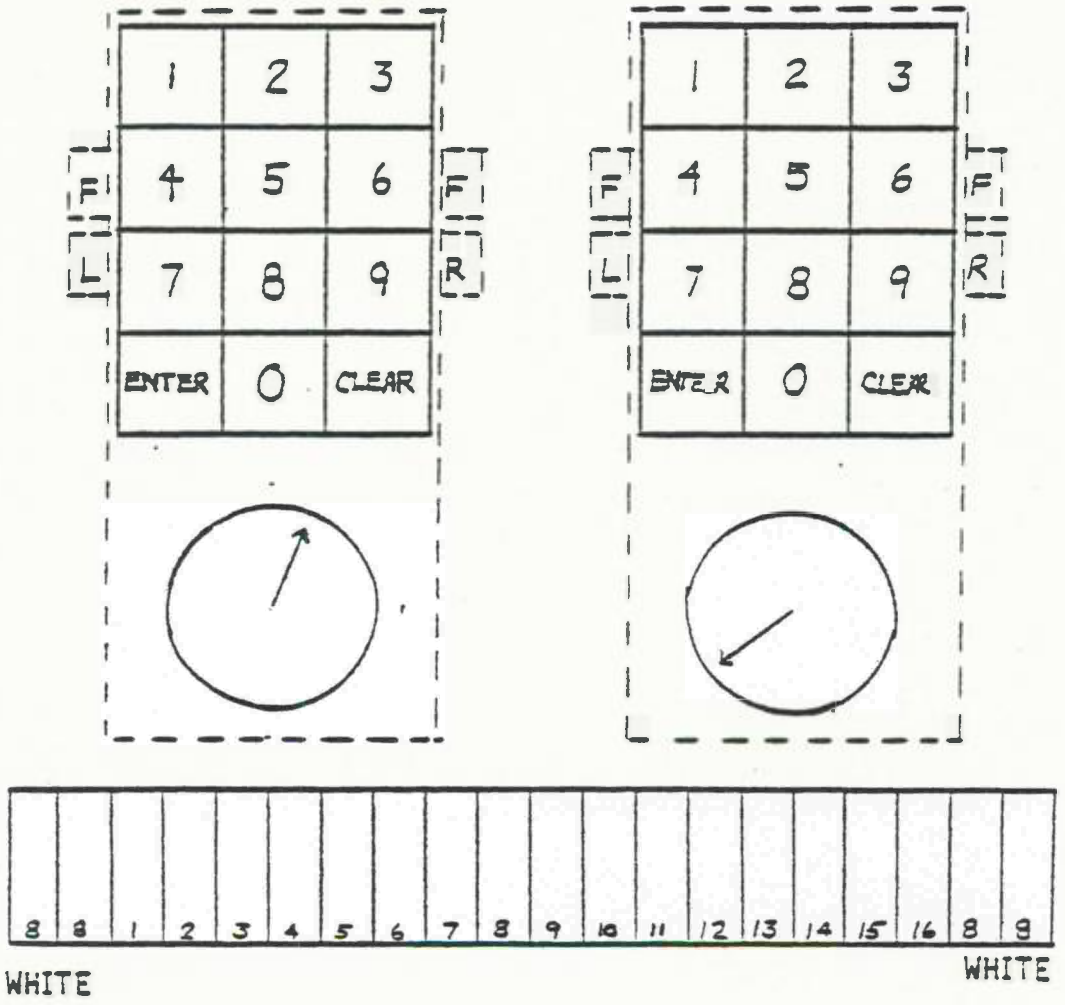
7. The next test is to check for the display of "F/B" and "VIS" to be alternately flashing. Depression of the clear button accepts the test. Depression of the enter button fails the test.

8. The successful end of the test will transfer control to the Baseball Cartridge. Observe title page. Press disc, note dispersal of players. Make one pitch, move the catcher, reset, observe title page. If any anomalies are noted during this entire sequence, the chip set fails.

9. If a failure has occurred in any step of the program, replace the chip indicated to have failed until the system passes as per Step 7 above.

STIC IMI ERROR CODE STATEMENT LIST

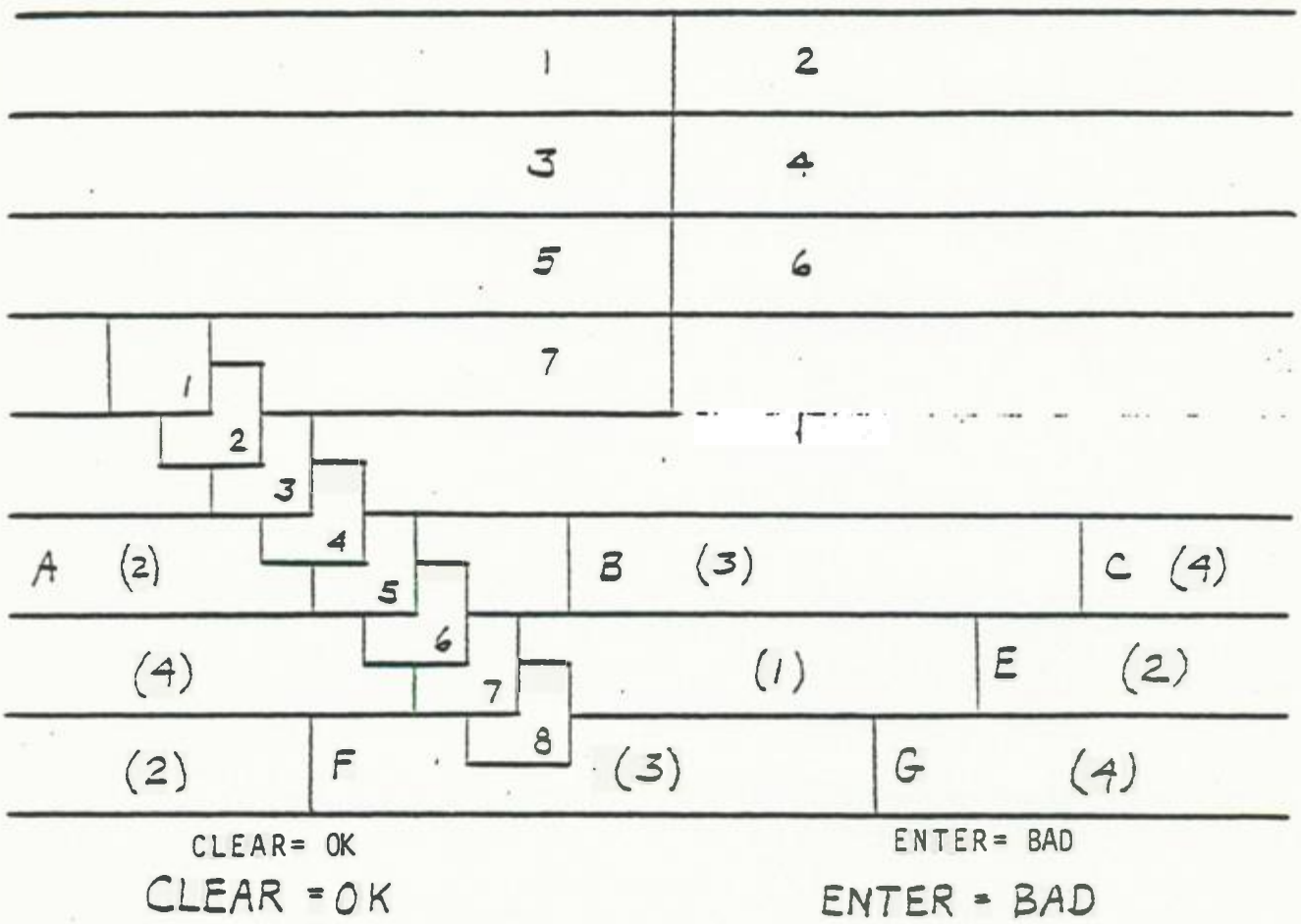
CODE	FAILURE MECHANISM
A	GROM checksum error
B	Low 2K executive ROM checksum failure
C	High 2K executive ROM checksum failure
D	STIC memory failure
E	Memory Failure - low order GRAM
F	Memory Failure - high order GRAM'
G	9600 Memory Failure
H	Scratchpad Memory Failure
J	8914 Memory Failure
K	Interaction Test
M	Type of 9502 and 9504 mismatch
N	Object not displaying completely
O	Colored squares quadrant select fail
P	Offset test fail
Q	Zoom in X fail
R	Zoom in Y fail
S	Mirror in Y fail
T	Mirror in X fail
U	Full/half height fail
V	8/16 line sequence fail
W	Background color stack, moving object priority, colored square fail, (operator decision)
X	Sound quality (operator decision)
Y	Visible/Invisible, foreground priority (operator decision)
Z	Mode One/Mode Two (operator decision).



COLOR BAR GENERATION

1. Black
2. Blue
3. Red
4. Tan
5. Grass Green
6. Green
7. Yellow
8. White
9. Gray
10. Cyan
11. Orange
12. Brown
13. Magenta
14. Lt. Blue
15. Yellow Green
16. Purple

FIGURE 1



COLOR CHECK

1. Black
2. Blue
3. Red
4. Tan
5. Grass Green
6. Green
7. Yellow
8. White

FIGURE 2

2	6	2	1	2	5	2	6
6	5	6	5	5	5	5	5

2	5	2	1	2	1
7	5	7	5	6	5

ALTERNATELY FLASHING
"MODE TWO"

COLOR CODES

1. Black
2. Blue
3. Red
4. Tan
5. Grass Green
6. Green
7. Yellow
8. White

FIGURE 3

REVISIONS

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
				Company Confidential			
C	5/7/82	13103		REWRITTEN			

GI DRAWING
AND SPEC. CONTROL
VALID COPY

SHEET	1	2	3	4	5	6	7	8					
LAST REV	C	C	C	C	C	C	C	C					

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT

MICROELECTRONICS GROUP

PLANT

MODULE

OPERATION

TITLE

RO-3-9505 CUSTOMER PROCUREMENT SPEC.
(40K) CARTRIDGE

	WRITTEN	APPROVED					
BY	G.D.H.	KQ	[illegible]	[illegible]	[illegible]		[illegible]
DATE	4/29/82	4/29	5/1/82	5/5/82	[illegible]		4/29/82

SHEET 1 OF 8

SPEC. NO. CPS-10047

REV C

1.0 SCOPE

This Customer Procurement Specification (CPS) covers the RO-3-9505 MOS ROM I.C

2.0 CIRCUIT FEATURES

- Mask programmable storage providing 4096 X 10 bit words.
- 16 bit on-chip address latch
- Control decoder
- Programmable memory map circuitry to place 4K ROM page within 65K word memory space located on 4K page boundaries.

3.0 AMENDMENTS

This CPS may only be amended by a written agreement between the parties.

4.0 ELECTRICAL ACCEPTANCE SPECIFICATION

The circuit must function within the range of electrical parameters given in this CPS.

5.0 CIRCUIT REQUIREMENTS

The RO-3-9505 operates as the program memory for systems using a CP1600 series microprocessor.

It is configured as 4096 X 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

6.0 OPERATING DESCRIPTION

The 9505 contains a programmable memory map location for its own 4K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9505 will output 10 bits of addressed data and also drive a logic zero on the top 6 bits of the bus.

6.1 INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	-
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	-
1	1	0	DW	-
1	1	1	INTAK	BAR

7.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Temperature Under Bias	0°C to +100°C
Storage Temperature	-55°C to +150°C
All Input or Output Voltages with respect to Vss	-0.2V to +9.0V
Vcc with respect to Vss	-0.2V to +9.0V

*Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATIONAL SPECIFICATION

Ambient Temperature 0°C to +55°C

D.C. CHARACTERISTICS

Vcc= +4.85 to +5.15V, Vss = 0.0V

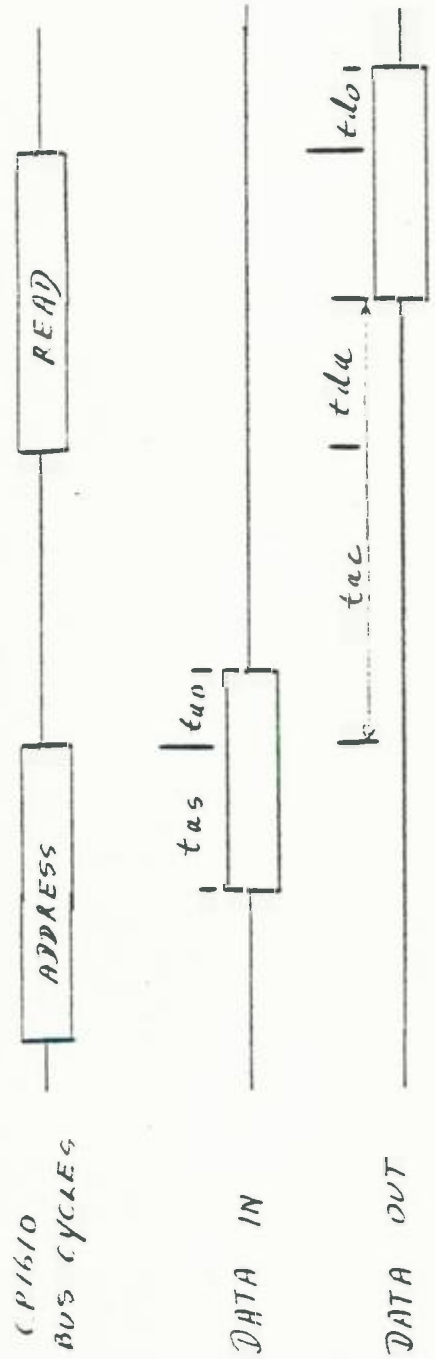
CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Input Logic Low	VIL	0	0.7	Volts	
Input Logic High	VIH	2.4	Vcc	Volts	
Input Leakage	IIL	-	5	uA	VIN = 0V to Vcc
CPU Bus Outputs					
Output Logic Low	VOL	0	0.5	Volts	IOL = 1.5mA]
Output Logic High	VOH	2.4	Vcc	Volts	IOH = 80uA] +150pf
Supply Current					
Vcc Supply	Icc	-	75	mA	at +55°C

A.C. CHARACTERISTICS

CHARACTERISTIC	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address Set Up	tas	300		nSec	
Address Overlap	tao		65	nSec	
CPU Bus Ouputs					
Turn ON Delay	tda	-	350	nSec	
Turn OFF Delay	tdo	80	250	nSec	
Access Time	tac		1.5	uSec	

Note: Input capacitance of all logic pins, 10pf max VIN=0V @ 1MHz
Not measured during production test.

MEMORY TIMING

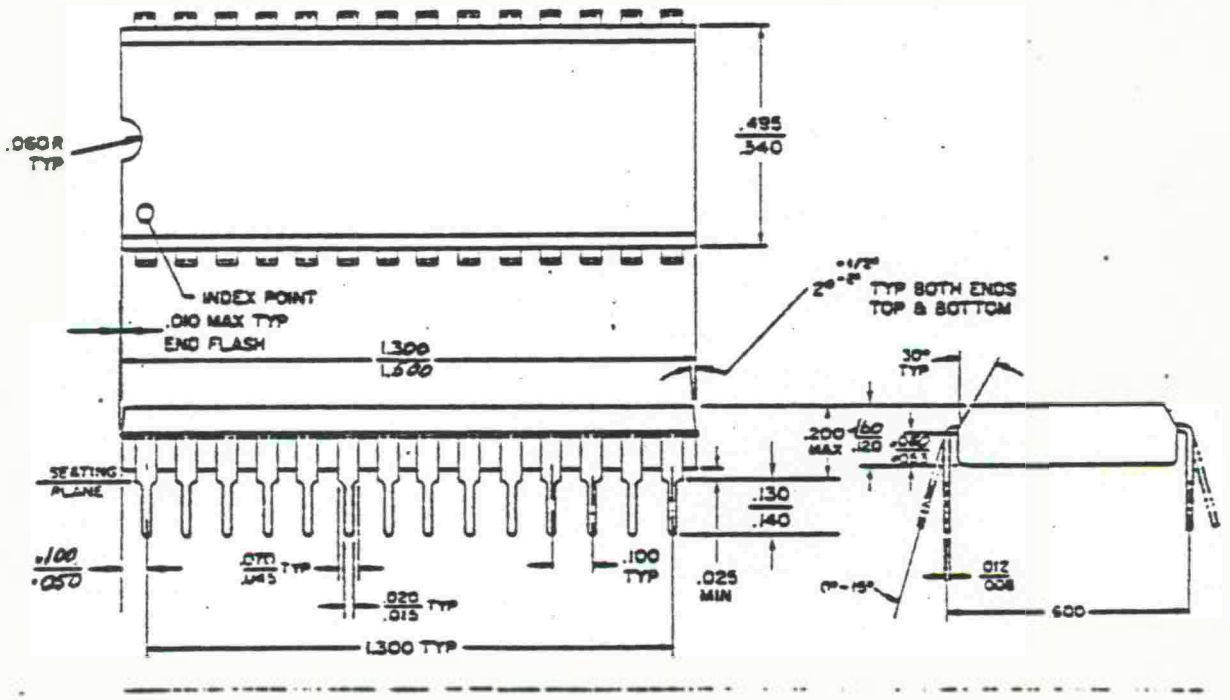


8.0 PIN CONNECTIONS

1	VCC	15	Vss
2	No Connection	16	DB7
3	No Connection	17	DB6
4	DB15	18	No Connection
5	No Connection	19	DB5
6	DB14	20	DB4
7	DB13	21	DB3
8	DB12	22	No Connection
9	DB11	23	DB2
10	DB10	24	DB1
11	No Connection	25	DB0
12	DB9	26	BDIR
13	DB8	27	BC2
14	No Connection	28	BC1

9.0 MECHANICAL CHARACTERISTICS

9.1 PACKAGE DIMENSIONS



9.2 SOLDERABILITY

The pins on this integrated circuit package meet solderability as given in MIL-STD-883B Method 2003.2 with the exception of Paragraph 3.2, Aging.

EXHIBIT C

Shipment Schedule: Game Sets and Cartridge Sets (000)

	GAME SETS				CARTRIDGE SETS			
MONTH	Min.	Cum.	Max.	Cum.	Min.	Cum.	Max.	Cum.
1981 Nov.	175	175	175	175	1100	1100	1100	1100
Dec.	150	325	175	350	700	1800	950	2050
1982 Jan.	125	450	175	525	400	2200	750	2800
Feb.	175	625	200	725	700	2900	1200	4000
Mar.	175	800	225	950	700	3600	1200	5200
Apr.	175	975	225	1175	700	4300	1200	6400
May	175	1150	235	1410	500	4800	1200	7600
June	175	1325	235	1645	500	5300	1200	8800
July	175	1500	230	1875	500	5800	1000	9800
Aug.*	165	1665	230	2105	400	6200	700	10500
Sept.	170	1835	235	2340	300	6500	700	11200
Oct.	165	2000	235	2575	300	6800	600	11800

*All Cartridge Set orders scheduled for shipment after August 1, 1982 will be completed with the shipment of one 40K ROM, except as otherwise requested by Buyer.

EXHIBIT D

MICROELECTRONICS GROUP

QUALITY CONFORMANCE REQUIREMENTS

EXHIBIT D

MICROELECTRONICS GROUP

QUALITY CONFORMANCE REQUIREMENTS

GROUP C - DIE - RELATED QUALIFICATION PROCEDURE (EVERY SIX MONTHS PER GENERIC CATEGORY)

TEST	REFERENCE MIL-STD-883 METHOD AS SPECIFIED	G.I. SPECIFICATION	CONDITIONS	LTPD
1. Operating Life	1005	Reliability testing performed by generic device per PSI	1000 hours per max. spec temp. 40 C	*15 Accept
OR				
HTRB	1015			
2. Endpoint Electrical		Per Customer Procurement Specification		

* Acceptance Criteria Based on Sample Being Prior Conditioned by 24-Hour Operation in This Same Electrical Circuit at 95 C and Resulting Infant Mortality Failures Removed From Sample.

MICROELECTRONICS GROUP

QUALITY CONFORMANCE REQUIREMENTS

GROUP D - PACKAGE RELATED QUALIFICATION PROCEDURE (EVERY TWELVE MONTHS PER GENERIC CATEGORY)

TEST	REFERENCE MIL-STD-883 METHOD AS SPECIFIED	G.I. SPECIFICATION	CONDITIONS	LTPD
Subgroup 1				
1. Solderability	2003	QCI 31003	Soldering Temperature	15
Subgroup 2				
1. Lead Fatigue	2004	QCI 31004	6 random leads 3 bend cycles Force: 8 oz, z1 apply 0.12" from bend radius	15 Accept 2
2. Lead Pull	2004	QCI 31002	6 random leads A tension of 8 oz	15 Accept 2
Subgroup 3				
1. Therm. Shock	1011	QCI 31011	10 cycles 0 C to 100 C Elect. Continuity test before and after test	15 Accept 2
2. Temp Cycle	1010	QCI 31010	10 cycles -65 C to 150 C Elect. Continuity test before and after test	15 Accept 2

MICROELECTRONICS GROUP

QUALITY CONFORMANCE REQUIREMENTS

GROUP D - PACKAGE RELATED QUALIFICATION PROCEDURE (EVERY TWELVE MONTHS PER GENERIC CATEGORY)

TEST	REFERENCE MIL-STD-883 METHOD AS SPECIFIED	G.I. SPECIFICATION	CONDITIONS	LTPD
Subgroup 3				
3. Pressure Cooker		QCI 30029	1 hr. min., 20 PSIG 115 C elect. readout before and after test	15 Accept 2
4. Moisture Resistance (Optional in lieu of Item 3, Subgroup 3)	1004	QCI 31001	25 C to 65 C, 90% humidity 3 hrs @ 65 C, 10 cycles	30 Accept 1
5. Endpoint Electrical			Per Customer Procurement Specification	

EXHIBIT E

Procedure for Handling Requests for Return of Rejected Products from Buyer's Subcontractors and MEL:

1. Once a month Buyer and Seller shall meet to inspect and verify the test equipment calibration and procedure at Buyer's subcontractors and MEL. If, during the term of this Agreement, Seller verifies that on a continual basis more than 10% of the individual units of the Products rejected by Buyer meet the Specifications, the parties will confer to develop the corrective action to be taken.

2. Buyer (Mattel/California) may request RMA numbers from Seller (Hicksville) on the first and third Mondays of each month (or more frequently if required) for all Buyer's "ship to" destinations. Each RMA request will contain the following information:

   (a) Part numbers of the rejected Products.

   (b) Reason for failure.

   (c) Date code of the Product(s) to be returned.

   (d) Quantity of Game Sets, Cartridge Sets or individual parts, whichever is applicable, to be returned.

   (e) Location from which rejected Products are to be returned, Radofin, Grandex or MEL and/or other sources as may be created.

   (f) If Products rejected at Buyer's incoming inspection, purchase order number against which rejected Products were shipped.

3. Seller will process the RMA request and advise Buyer (Mattel/California) within five (5) business days of the RMA number and, if applicable, the "ship to" destination of the rejected Products.

4. Shipping instructions for Taiwan (Grandex) will be as follows:

   (a) Grandex will, via telex, inform Buyer (Mattel/Calfornia) and Seller (Kaohsiung and Hicksville) of RMA number, ship date, waybill, quantity, part number and method of shipment.

   (b) Seller (Kaoshiung) will generate a proforma invoice to clear Products through Taiwan customs.

   (c) Rejected Products are to be returned freight collect.

   (d) Grandex will endeavor to ship rejected Products within

ten (10) days after issuance of an RMA number. Seller will not be required to ship replacement Products until rejected Products are received.

5. Shipping instructions for Hong Kong (MEL and Radofin) will be as follows:

   (a) Seller (Hong Kong) will pick up the rejected Products within five (5) business days after issuance of RMA number. If rejected Products are not picked up within said five (5) business days, Products may be returned to Seller (Kaoshiung) freight collect.

   (b) Seller (Hong Kong) will generate a proforma invoice to clear Products through Taiwan customs and return the rejected Products to Kaohsiung.

6. Rejected Products (and only the rejected parts in a kit) will be labeled or coded by each subcontractor or MEL to indicate point in the test cycle at which Products failed. Labeling or coding should not obstruct legibility of date code.

7. Buyer (Mattel/California) will promptly issue a replacement order for all Products returned under an RMA number at time RMA number is issued by Seller.

8. The unit price applicable to rejected Products and the related debits, credits, replacement orders and rebillings will be governed by Note 8 of Exhibit A. All debits and credits to be exchanged between Buyer (Mattel/California) and Seller (Hicksville) only.

EXHIBIT F

(1) General Instrument Mask Numbers Covered by Paragraph 12:

- 30203 (CPU)
- 32040 (RAM)
- 32024 (STIC-U.S.)
- 32027 (STIC-EUROPE)
- 32025-XXX (20K (Low) Exec.ROM)
- 32038-YYY (20K (High) Exec.ROM)
- 32026-003 (Graphics ROM)
- 32035 (Color)
- 32022-115 (Sound)
- 32038-XXX (20K Cartridge ROM)
- 32046-XXX (40K Cartridge ROM)
- 32121-AAA (40-1/4K Exec. ROM)

(2) Royalties To Be Paid By Mask Number In (1) Above On Sales By Each Second Source:

- First $2 million	7-1/2%
- Next $2 million	5%
- Thereafter for all sales through 12/31/84*	2-1/2%

*After 12/31/84, no further royalties will be payable.

(3) Technical Information to be Supplied Pursuant to Paragraph 12:

- Calma tapes
- Sentry Test Tapes, Sentry Load Board Drawings or Test Program (specifications if tapes are not available for subcontractor test equipment).
- Customer Procurement Specifications
- Process Parameter Specifications
- Marking and Bonding Diagrams

(4) Additional Technical Information to be Supplied Pursuant to Paragraph 12(d)

- Timing and Logic Diagrams

SYM	DATE	CN	SHT	DESCRIPTION	BY	CH	APP
A	10-26-81			Release - Typed on Lanier Disk 32 (PP)	PP		ES

SPI-

EXHIBIT G

GI DRAWING
AND SPEC. CONTROL
VALID COPY

SHEET	1	2	3	4									
LAST REV	A	A	A	A									

SHEET													
LAST REV													

DISTRIBUTION LIST

SUPERSEDES

SUPERSEDED BY

GENERAL INSTRUMENT

MICROELECTRONICS GROUP

PLANT

MODULE

TITLE WEEKLY BURN-IN OF KEY PRODUCTS

OPERATION

	WRITTEN	APPROVED						SHEET 1 OF 4	
BY	David C. [illegible]		BDR	[illegible]				SPI- 44526	REV A
DATE	10-30-81		11-3.	11-5-81					

FORM SPI-1 (2/81)

TITLE:	WEEKLY BURN-IN OF KEY PRODUCTS	SPI NO.:	44526
WRITTEN BY:	Group Staff	EFFECTIVE:	10/26/81
APPROVED BY:	Group Staff	REVISED:	

1.0 PURPOSE

To provide a consistent procedure for the weekly burn-in of Key Products.

2.0 SCOPE

Microelectronics Front End Facilities, worldwide.

3.0 PROCEDURE

3.1 It is important to provide a consistent weekly measure of key product reliability.

3.2 The weekly measure will consist of a full functional stress at an elevated temperature, typically 125°C, unless design/packaging considerations dictate a lower temperature.

3.3 Every week a sample of 54 units that have passed final test will be randomly drawn from recent production and placed on test.

3.4 Readouts will be done at 24 $\pm$ 2 hours and 168 $\pm$ 4 hours.

3.5 Functionally failed (not DC) units at 24 hours will be left in test and retested as part of the 168 hours test. Fails at 168 hours will be sent to failure analysis for electrical and physical failure analysis. A monthly tabulation of the key modes of failure will be issued as part of the Quality Manager's Letter.

3.6 The data from the weekly burn-in will be reported on a monthly basis as part of the Quality Manager's Letter. Two charts will be provided:

1. Cumulative percent fallout at 24 hours versus week periods.

2. The failure rate from 24 to 168 hours (%/K Circuit Hours). The failure rate is estimated by the following equation:

$$FR\ (\%/Khr) = \frac{n_d \times 10^5}{144 \times N - 72 \times n_d}$$

Where:

n_d = Number failing at 168 hours minus number failing at 24 hours.

N = Number surviving at 24 hours.

This failure rate is plotted versus the same week periods as in Chart Number 1.

The 24 hour readout will provide a measure of the early fail portion (infant mortality) of the bathtub (instantaneous failure rate versus time) curve. The second curve will provide between 24 to 168 hours an estimate of the flat (constant) failure rate portion of the bathtub curve.

An example of the plots is attached (Figure No. 1).

3.7 The stressing will be done on key "bell weather" products as specified either by CPS or by Management. Normally, the key products will be the high volume items for a wafer module. It is anticipated that, typically, there will be only one or two such "bell weather" products per plant and that they will remain the same products over extended periods so that a cohesive history is obtained.

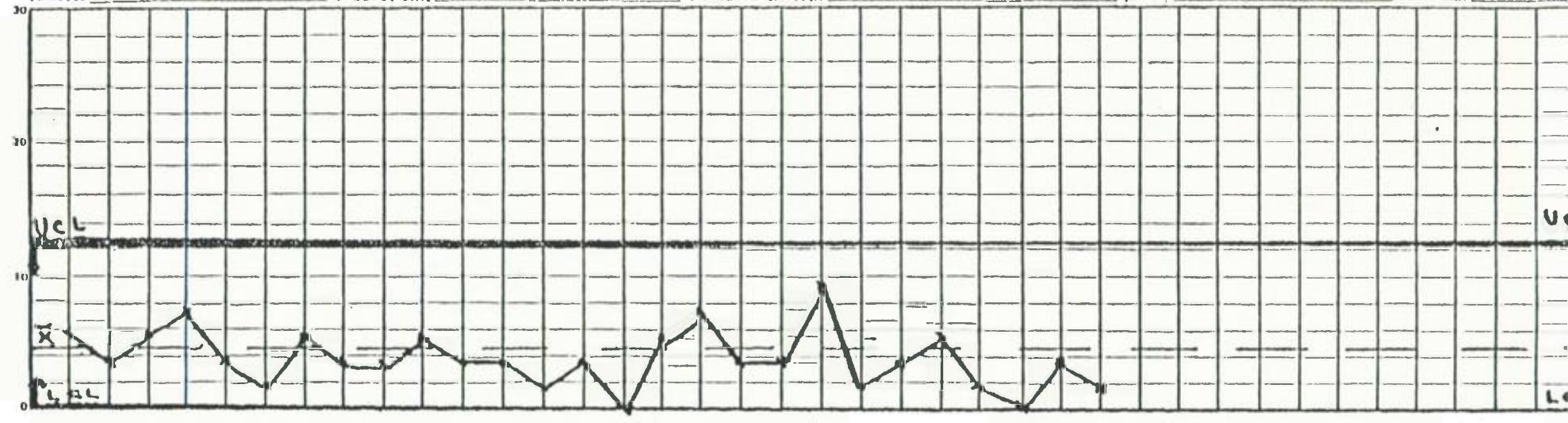
4.0 RESPONSIBILITY

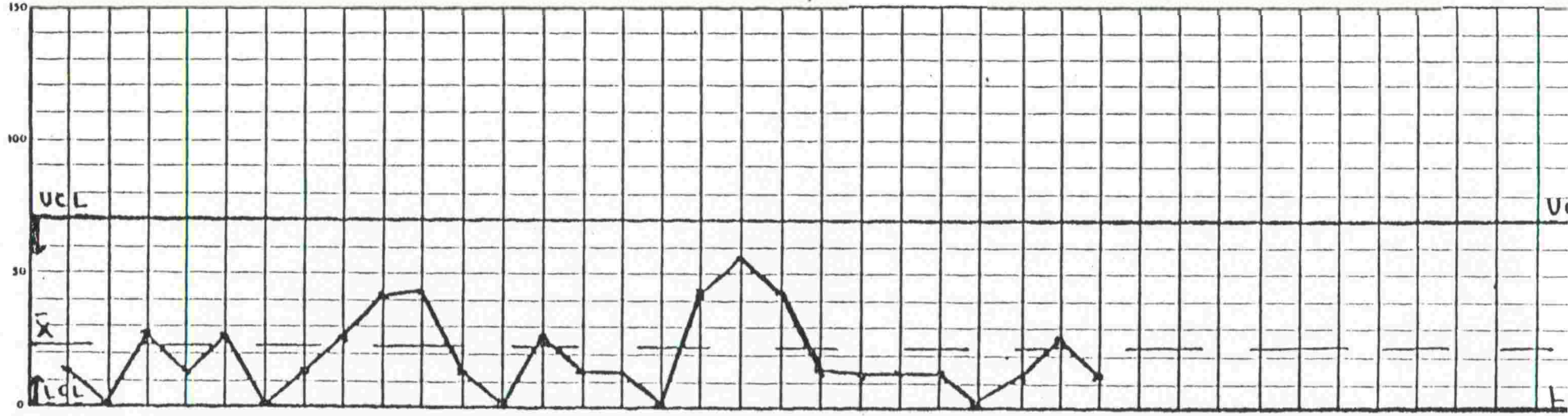
4.1 It is the responsibility of Quality Control at each front end facility to perform the weekly burn-in and assure that the correct procedures are followed.

GENERAL INSTRUMENT

PROCESS CONTROL CHART

PROCESS P-EAROM PRODUCT LINE MASK # 8231 MEASURED CRITERIA BURN-IN FAILURES PERIOD FEB. 1981 CHART NO. 1





Week Code	8105	8106	8107	8108	8109	8110	8111	8112	8113	8114	8115	8116	8117	8118	8119	8120	8121	8122	8123	8124	8125	8126	8127	8128	8129	8130	8131
Sample Size	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51	51
24 Hrs.																											
Cum. # Failure	3	1	3	4	2	1	3	2	2	3	2	2	1	2	0	3	4	2	5	5	1	2	3	1	0	2	1
Cum. % Failure	5.6	1.9	5.6	7.7	3.8	1.9	5.6	3.8	3.8	5.6	3.8	3.8	1.9	3.8	0	5.6	7.7	3.8	9.7	9.7	1.9	3.8	5.6	1.9	0	3.8	1.9
168 Hrs.																											
Cum. # Failure	4	2	5	5	4	1	4	4	5	6	3	3	3	3	1	7	7	6	9	6	2	3	4	1	1	4	3
Cum. % Failure	7.4	3.7	9.3	9.3	7.4	1.9	7.4	7.4	9.3	11.1	5.6	5.6	5.6	5.6	1.9	13.0	13.0	11.1	17.3	11.1	3.7	5.6	7.4	1.9	1.9	7.4	5.6
Failure Rate	11.8	0	20.8	19.2	17.6	0	13.8	13.8	19.6	19.2	13.2	13.2	13.0	13.2	0	26.0	26.0	22.6	34.6	22.6	7.8	13.2	17.6	4.0	0	17.6	13.2

BASED ON WEEK CODES 8105-8124:

CUM. % FAILURES AT 24 HRS.

AVERAGE = $\bar{X}$ = 4.4%

STD. DEV = $\sigma = \sqrt{\frac{4.4(95.6)}{51}}$ = 2.8%

UCL = $\bar{X}$ + 3σ = 12.8%

LCL = $\bar{X}$ - 3σ = 0%

FAILURE RATE FROM 24 TO 168 HRS.

AVERAGE = $\bar{X}$ = 21.4% PER K CIRCUIT HRS.

STD. DEV. = σ = 16.3%

UCL = $\bar{X}$ + 3σ = 70.3%

LCL = $\bar{X}$ - 3σ = 0%

SPI-44526 REV A SHEET 4

EXHIBIT H

QUALITY AND RELIABILITY PROGRAM CONTAINED IN THE "MATTEL/GENERAL INSTRUMENT DISCUSSIONS" (BLACK BOOK) DATED DECEMBER 1, 1981

MATTEL/GENERAL INSTRUMENT

QUALITY AND RELIABILITY PROGRAM

November 1981 through May 1982

OBJECTIVES

- Reduce kit incoming inspection rejection rate to 1%.
- Reduce Mattel kit assembly/test/burn-in fallout to 5% of kits accepted.
- Reduce post Mattel burn-in operational failures, due to LSI kit, to 3%.

PRESENT STATUS

Gross (that is "non-failures," and assembly/test damage not removed from numbers).

- Kit Incoming Inspection 2%.
- Kit Assembly/Test/100% Burn-in fallout 18%.
- Reported Post Burn-in Operating Failures due to LSI kit 6%.

(REFERENCE EXHIBITS I THRU VII ATTACHED).

PROGRAM MANAGER

- Bob Jones (career history, Exhibit VIII).
- Full time until objectives are achieved.

MAJOR SUPPORT ASSIGNMENTS

- Dave Trindade and Al Adell for design of experiments.
- Bill Churchill for Chandler detailed follow.
- Roland Henderson for Mattel detailed follow.
- Bill Giles for Kaohsiung detailed follow.

PROGRAMS

- PROGRAM A - KIT INCOMING INSPECTION — Intent is to eliminate need for kitting by having all parts totally interchanged
  - Eliminate IMI as a 100% final test/kitting requirement

CORRECTIVE ACTION PROGRAM

INCOMING KIT REJECTION RATE - 2%

CAUSE: MANUAL (IMI) TESTING/CORRELATION

	PROJECT	RESPONSIBILITY	COMPLETION DATE
A.1	REVISE CPS'S	*D. HARROWER	FEBRUARY 1, 1982
A.2	REVISE SENTRY PROGRAMS		
	RAM	W. CARTER	MARCH 1, 1982
	STIC (DEFINITION)	R. SIMON	FEBRUARY 1, 1982 (TASK
	CPU	L. ROZEK	MARCH 1, 1982 DEFINITION)
	ROMs - PROGRAM	E. NEWTON	MAY 1, 1982
	ROMs - GRAPHICS	E. NEWTON	JUNE 1, 1982
	SOUND CHIP	W. CARTER	MAY 1, 1982

*Direct test program modification effort

A.3	IMI FAILURE/CORRELATION	W. GILES	ON-GOING WITH THE ABOVE
	REWORK/MODIFICATION	ABOVE	AS REQUIRED IN APRIL-SEPTEMBER TIME PERIOD

• PROGRAM B - KIT ASSEMBLY/TEST/100% BURN-IN FALLOUT

- HARD FAILURES (PROJECT B.1)

CORRECTIVE ACTION PROGRAM

HARD FAILURES - 41% OF TOTAL CHIP FAILURES

CAUSE: WORKMANSHIP DEFECTS - PRIMARILY METAL DAMAGE (75% OF TOTAL)

	PROJECT	RESPONSIBILITY	COMPLETION DATE
B.1.1	IMPLEMENT IMPROVED WAFER PACKING AND SHIPPING TO KAOHSIUNG	C. STOCKSON	11/30/81
B.1.2	DETERMINE SOURCE OF METAL DAMAGE BY PROCESS STEP (See action plan attached)	F. STRNAD/ F. HALLMAN	11/30/81
B.1.3	IMPLEMENT CORRECTIVE ACTIONS REQUIRD IN WAFER MODULES	M. STRNAD/ F. HALLMAN	01/04/82
B.1.4	DETERMINE SOURCE OF METAL DAMAGE AFTER WAFER PROCESSING	C. STOCKSON	12/01/81
B.1.5	IMPLEMENT CORRECTIVE ACTION REQUIRED - PROBE, SHIPPING, KAOHSIUNG ASSEMBLY (See action plan attached)	C. STOCKSON	12/30/81
B.1.6	MONITOR METAL DAMAGE AT CHANDLER AND KAOHSIUNG TO DETERMINE QUANTITATIVE IMPROVEMENT	C. STOCKSON - CHANDLER W. GILES - KAOHSIUNG	--CONTINUOUS--

CORRECTIVE ACTION PROGRAM

HARD FAILURES - CONTINUED

	PROJECT	RESPONSIBILITY	COMPLETION DATE
B.1.7	EFFECTUATE CORRECTIVE ACTIONS BETWEEN KAOHSIUNG, CHANDLER, HONG KONG, TAIPEI FOR OTHER WORKMANSHIP PROBLEMS; TEST, ASSEMBLY DIE RELATED	R. JONES/ R. HENDERSON	CONTINUOUS
B.1.8	PILOT LOT 100% AND 200% VISUAL SCREENED TO QCI 30014 and 30053 AND KEPT SEPARATE BY "RED DOTTING" THROUGH MATTEL ACCEPTANCE THROUGH SHIPMENT CYCLE. IF RESULTS OF EXPERIMENT #10 ARE POSITIVE, FURTHER TIGHTEN PRE-CAP VISUAL SCREEN (LABOR RESOURCES AND EQUIPMENT WILL BE SUPPLIED).	W. GILES/ D. TRINDADE	3/15/82

- SOFT FAILURES (PROJECT B.2)

CORRECTIVE ACTION PROGRAM

SOFT FAILURES - 42% OF TOTAL CHIP FAILURES

CAUSE: EXPOSED GATE OXIDES - POOR OVERCOAT INTEGRITY

	PROJECT	RESPONSIBILITY	COMPLETION DATE
B.2.1	PRELIMINARY EVALUATION OF FLOOD IMPLANT TO ELIMINATE EXPOSED GATE OXIDE PROBLEM (See action plan attached)	R. MUSA	11/30/81
B.2.2	IMPLEMENT FLOOD IMPLANT FOR STIC AND RAM	M. STRNAD	03/01/82
B.2.3	DEFINE AND ESTABLISH ON-GOING MONITOR FOR PYRO INTEGRITY (See action plan attached)	W. CHURCHILL	COMPLETE (QCI 30343)
B.2.4	DETERMINE CAUSE AND REQUIRED PROCESS MODIFICATIONS TO PASS PYRO INTEGRITY TEST	M. STRNAD/ F. HALLMAN	12/18/81
B.2.5	IMPLEMENT PROCESS FOR IMPROVED PYRO	M. STRNAD/ F. HALLMAN	01/04/82
B.2.6	DESIGN AND TOOL DETECTOR CIRCUITS IN EACH DIE OF 32040 TO SCREEN MISALIGNMENT ELECTRIALLY	D. BUTLER	11/11/81
B.2.7	EVALUATE TEST PROCEDURE FOR SCREENING	R. MUSA	12/28/81
B.2.8	INCREASE BURN-IN POSITIONS	W. CHURCHILL	300 12/01/81 600 02/01/82

CORRECTIVE ACTION PROGRAM

SOFT FAILURES - CONTINUED

	PROJECT	RESPONSIBILITY	COMPLETION DATE
B.2.9	PREPARATION OF A NUMBER OF KITS WITH STIC/RAM IN NITRIDE OVERCOAT KEPT SEPARATE BY "YELLOW DOT" THROUGH MATTEL ACCEPTANCE THROUGH SHIPMENT CYCLE	M. STRAND/ D. TRINDADE	3/1/82
B.2.10	PREPARATION OF A NUMBER OF KITS WITH STIC/RAM IN HERMETIC PACKAGES (SAME TEST CYCLE - "BLUE DOT").	W. GILES/ D. TRINDADE	3/1/82
B.2.11	EVALUATION OF A NUMBER OF KITS WITH STIC/RAM BURNED IN (SAME TEST CYCLE - "RED DOT").	R. HENDERSON	1/15/81 FOR THE PRESENT TEST OF 2600 DEVICES STIC, RAM, CPU
B.2.12	PREPARATION OF A NUMBER OF KITS WITH STIC/RAM IN LOW CHLORINE COMPOUNDS (SAME TEST CYCLE - "WHITE DOT").	W. GILES/ D. TRINDADE	4/1/82

- TESTED/USED OUT OF CPS LIMITS (PROJECT B.3)

TESTED/ USED OUTSIDE C.P.S.

17% OF TOTAL CHIP FAILURES

C.P.S. REQUIRES CHIP SET TO FUNCTION IN 40 DEGREES CELSIUS AMBRIENT

G.I. TESTS INDIVIDUAL CHIPS ON AUTOMATIC TESTER AT TEMPERATURE EMPIRICALLY DETERMINED TO ASSURE 40 DEGREES CELSIUS CHIP SET IMI FUNCTION

MATTEL REQUIRES CHIP SET TO OPERATE IN INTELLIVISION WITH SEALED CHASIS AMBIENT - CHIP SET AT 50 TO 60 DEGREES CELSIUS AMBIENT

WC
12/1/81

TESTED/USED OUT OF CPS LIMITS (PROJECT B.3) - CONTINUED

	PROJECT	RESPONSIBILITY	COMPLETION DATE
B.3.1	RECALIBRATE INTELLIVISION OPERATING ENVIRONMENT	R. HENDERSON	12/3/81
B.3.2	RECALIBRATE CHIP "CPS AMBIENT" TO SUIT THE ACTUAL OPERATING ENVIRONMENT	R. HENDERSON	12/3/81
B.3.3	REDO CPS'S TO CONFORM TO THE ACTUAL OPERATING ENVIRONMENT	D. HARROWER	2/1/82
B.3.4	REDO COMUTER TEST PROGRAMS AND RAIL TEMPERATURES TO CONFORM	D. HARROWER & VARIOUS OTHERS	THRU 6/1/82

° PROGRAM C - POST BURN-IN OPERATING LIFE FAILURES

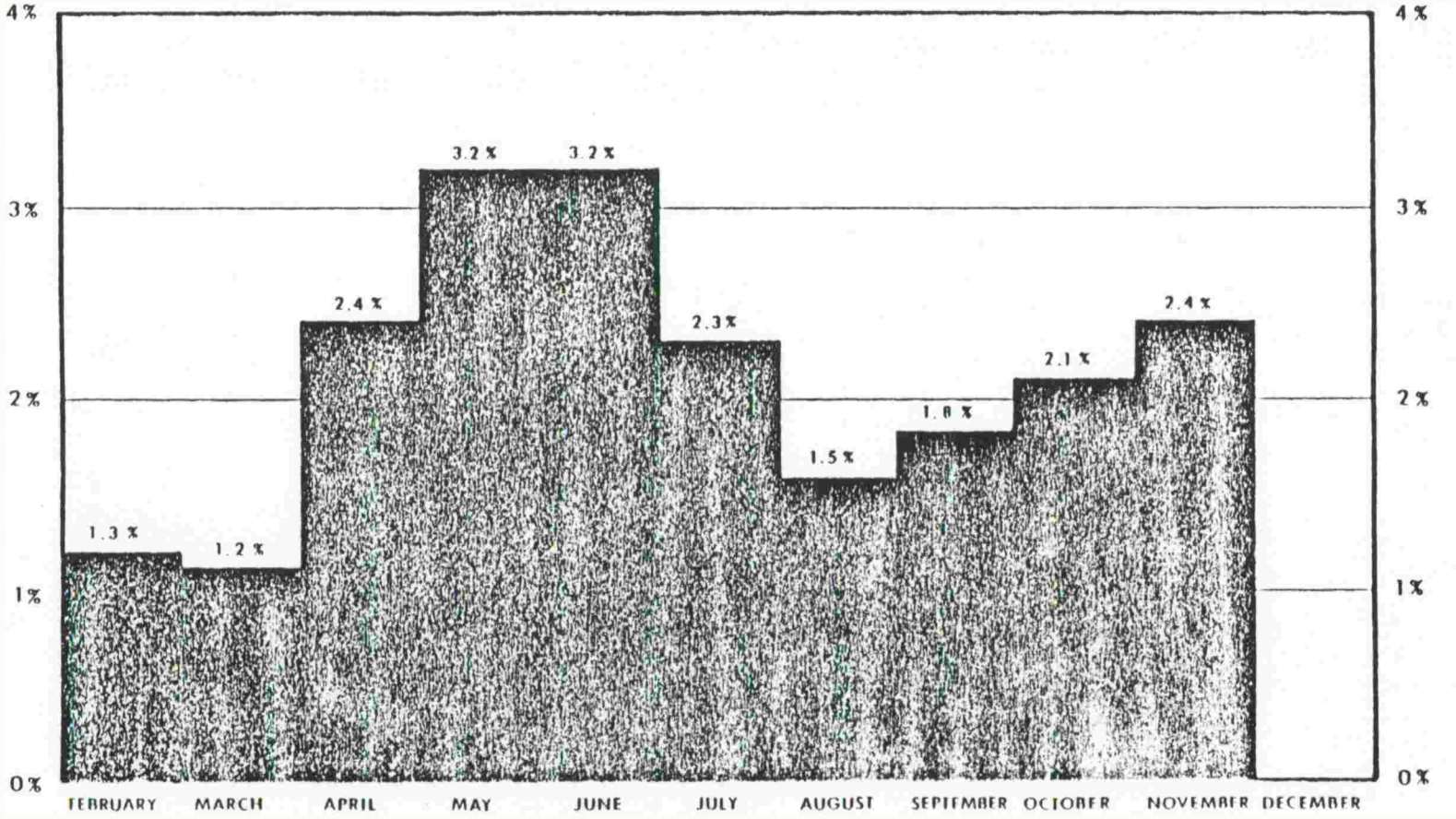
- ANALYZE FIELD RETURN REJECTS TO DETERMINE IF FAILURE MODALITY IS SIMILAR TO TO ASSEMBLY/TEST/100% BURN-IN MODALITY.

PROJECT	RESPONSIBILITY	COMPLETION DATE
C.1 MONTHLY RETURNS FROM MERC	R. HENDERSON	1/4/82 ON GOING
C.2 ESTABLISH MONTHLY REPORT (FIELD FAILURES AND DATE CODES)	R. HENDERSON	1/18/82
C.3 ESTABLISH ROUTINE ANALYSIS PROCEDURE (AND STAFFING)	W. CHURCHILL	1/4/82
C.4 ESTABLISH MONTHLY REPORT (FAILURE ANALYSIS MODALITY: FIELD AND INTERNAL)	W. CHURCHILL	2/1/82

EXHIBIT 1

MATTEL - INCOMING INSPECTION PERCENT DEFECTIVE KITS

QCI - 25



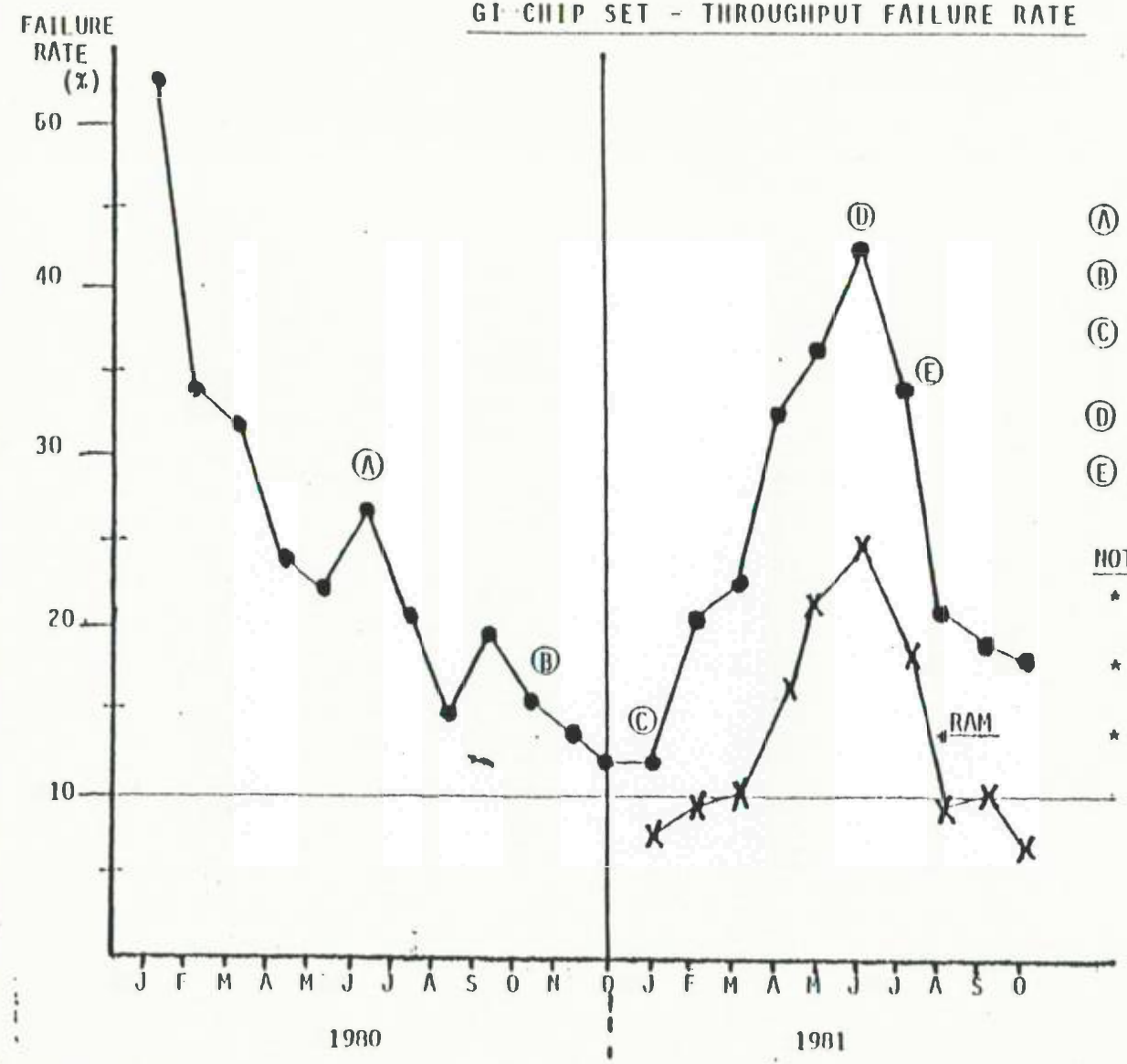
1981

W. CHURCHILL
NOV. 30, 1981

MATTEL ELECTRONICS

J. RALL
11/9/81
PA 503

GI CHIP SET - THROUGHPUT FAILURE RATE



ACTION KEYS

Ⓐ Task Force #1 Implemented

Ⓑ Removal 70°C Logic Board Test

Ⓒ Heat Spreader Added (RAM/STIC/CPU)

Ⓓ Task Force #2 Implemented

Ⓔ Removal of Heat Spreaders (RAM/STIC)

NOTES:

* Avg. "RAM" Fail. Rate (1/80-10/81) = 10.5%
* Avg. "STIC" Fail. Rate (1/80-10/81) = 5.7%
* Oct. Combined Failure Rate = 9.5%

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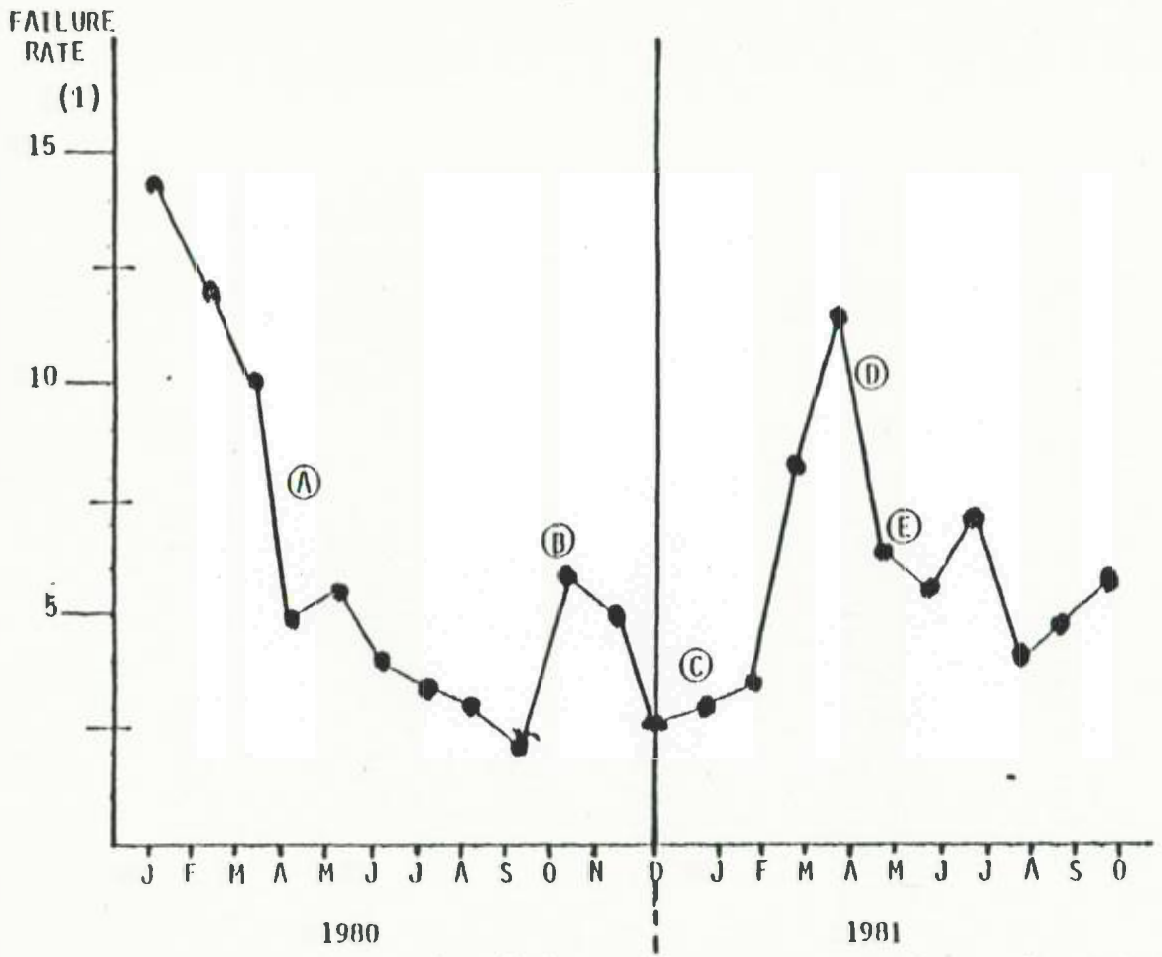
EXHIBIT III

MATTEL ELECTRONICS

J. RALL
11/9/81
PA 503

GI FAILURE RATE - MATTEL (500) HOUR LIFE TEST



ACTION KEYS

Ⓐ Task Force #1 Implemented

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Ⓔ Removal of Heat Spreaders (RAM/STIC)

NOTES:

* Avg. "RAM" Fail. Rate (1/80-10/81) = 10.5%
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* Oct. Combined Failure Rate = 9.5%

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EXHIBIT IV

LIFE TEST DATA

MATTEL

CONDITIONS: 25 DEGREES C - 500 HOUR - 6 HOUR PRE-SCREEN
(ENCLOSED GAME)

	JUN.	JUL.	AUG.	SEPT.	OCT.
RAM	2.0	3.7	1.0	1.5	2.0
STIC	1.0	1.0	1.0	2.0	1.5
TOTAL	6.5	7.3	4.5	5.0	5.3

KAOHSIUNG

CONDITIONS: 40 DEGREES C - NO PRE SCREEN
(OPEN GAME)

	JUL. - 1000 HR.	OCT. - 500 HR.
RAM	8.0	8.0
STIC	10.0	5.0
TOTAL	20.0	18.0

CHANDLER

CONTITIONS: 125 DEGREES C - NO PRE SCREEN - 100 HR. SIMILATED
APPLICATION

	MAY	JUN.	JUL.	AUG.	SEPT.
RAM	12.3%	9.3%	5.5%	2.5%	4.5%
STIC	5.5	2.7	2.4	1.0	2.3

WC/RH
12/1/81

EXHIBIT V

MATTEL IN-PROCESS KIT FALLOUT

TOTAL LINE KIT FALLOUT (83 PERCENT OF LOSS AT POST BURN-IN)		18 PERCENT
THROUGHPUT LOSS DUE TO FAILURE OF:		
RAM	LSI	40 PERCENT
STIC	LSI	30 PERCENT
CPU	LSI	12 PERCENT
SOUND	LSI	7 PERCENT
OTHER FOUR	LSI	11 PERCENT
		100 PERCENT

WC
12/1/81

EXHIBIT VI

ANALYSIS OF INDIVIDUAL LSI

LSI	HARD FAILURES	SOFT FAILURES	TESTED/USED BY CUSTOMER OUTSIDE OF CPS LIMITS	TOTAL
RAM	20%	60%	20%	100%
STIC	42%	42%	16%	100%
CPU	64%	16%	20%	100%
SOUND	88%	8%	4%	100%
OTHER FOUR	55%	25%	20%	100%

WC
12/1/81

EXHIBIT VII

MATTEL ELECTRONICS

J. RALL
11/9/81
PA 503

INTELLIVISION MASTER COMPONENT QUALITY

- Total Master Components Sold to Date (9/81) = 450,000
- Gross Returns to Date = 67,950
- Gross Return Rate = 15.1%

PRIMARY FAILURE MODES

- Hand Controller Related	=	3.2%	(14,400 Units)
- GI Chip Set Related	=	6.3%	(23,350 Units)
- All Other Failures	=	2.6%	(11,700 Units)
- Non-Defectives	=	3.0%	(13,500 Units)
TOTAL	=	15.1%	(67,950 Units)

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EXHIBIT VIII

RESUME

OF

ROBERT P. JONES

TELEPHONE: (201) 534-4716
Age: 50
Married, four children

SUMMARY:

Twenty-three years of semiconductor experience in manufacturing and operations management (Front-End/Back-End), manufacturing, process, product and design engineering functions.

EXPERIENCE:

General Instrument Corporation, Microelectronics Division
(1978 to Present)

Operations Manager, Hicksville Plant
(June 19, 1978 - Janaury 1, 1980)

Responsibilities: The coordination and direction of Back-End functions (Assembly, Test, Product Engineering, Customer Service, Production Control). During this tenure the coordination of these Back-End functions resulted in major organizational accomplishments through discipline with positive resulting customer satisfactions.

Plant Manager, Hicksville Plant
(January 1, 1980 - October 1, 1981)

Responsibilities: All site functions. Wafer Fab, Photomask, Assembly, Test, Product Engineering, Customer Service, Production Control. In addition, in the absence of the Vice President & Division General Manager, for a period of fourteen months while that Manager was on off-site assignment, the Plant Managers' position had the administrative responsibility of managing marketing, sales and design engineering.

Staff Assistant to the Deputy Group Executive
(October 1, 1981 - Present)

Responsibilities: Worldwide implementation, coordination and direction of new modular development, construction, process,activation and staffing for quality and productivity accomplishments.

RCA, Solid State Division
(1966 to 1978)

Director, MOS Engineering (Somerville, New Jersey)
(1 Year)

Responsibilities: Process development and improvement, package technology, test technology, and design automation. Major accomplishments: (a) directed a task force effort that within six months resolved a reliability problem existing for six years, (b) installed productivity measuring tools and discipline within the MOS engineering organizations (c) selectively reduced cycle time by a factor of 30%

Manager, Findlay Plant (Findlay, Ohio)
(2 Years)

Responsibilities: All location functions. Staff consisted of the following managers: MOS Wafer Fabrication, MOS Assembly and Test, MOS High Reliability Manufacturing, Stem Manufacturing, Materials Engineering, Purchasing, Quality & Reliability Assurance, Financial Operations, Industrial Relations and Plant Engineering. Location population: 1500. Major accomplishments: (a) plant management through the recession year of 1975 and rapid recovery year of 1976, (b) manufacturing cost reduction each year of 15% - 20%, and (c) reduction of manufacturing cycle times by 30% - 50%.

Manager, MOS Integrated Circuit Manufacturing
(6 Years)

Responsibilities: Two domestic MOS factories employing 900 personnel, start-up planning and facilitation for a third domestic location. Major accomplishments: Successful establishment and expansion of three MOS manufacturing operations.

Engineering Leader, MOS Design
(1 Year)

Responsibilities: Process development and device layout design for MOS circuits. Major accomplishment: successful program to take a troubled MOS product line from non-reproducible model shop status to going factory status.

Engineering Leader, Bipolar IC Manufacturing
(2 Years)

Responsibilities: Process engineering responsibility for wafer and assembly processes, and product engineering for a family of linear integrated circuits.

Philco-Ford, Semiconductor Division
(1960 - 1966)

Production Manager, Microelectronics Division
(2 Years)

ProjectEngineer - Silicon Planar Pre-Production Department
(2 Years)

Engineering Supervisor, Alloy Transistor Department
(2 Years)

Textile Machine Works, Wyomissing

Apprentice, Machinist, Toolmaker

EDUCATION:

Penn State University	1952 - 1955	BSME	(Honors)
Penn State University	Graduate Courses in Business and Industrial Engineering		

GENERAL INSTRUMENT

FY'82 ACTION PLANS

GROUP: MICROELECTRONICS

DIVISION: CHANDLER/PLANT 093

DEPT/PROJECT B.1.2

DATE: November 11, 1981

KEY RESULT OBJECTIVE:

Reduce wafer processing metal-related defects; reduce hard failure reliability problems.

QUANTITATIVE OBJECTIVE

TARGETED COMPLETION DATE
March 1, 1982

PRIME RESPONSIBILITY
M. Strnad/F. Hallman

TACTICAL ACTION PROGRAM:	DATE OF ACTION PLANNED	DATE OF ACTION TAKEN	STATUS/COMMENTS
1. Visual inspection of all concerned areas: Metal Photo, Metal Etch, Pyro, Pyro Photo, Pyro Etch, Alloy, HF Fume, Gold Back, Pre-Probe Inspection	11/20/81	11/20/81	Individual Responsibility: R. Ravindhran - Wafer C L. Wei - Wafer B
2. Determine major problem areas.	11/30/81	11/20/81	Pyro rocks, wafer handling, metal photo
3. Investigate best possible solutions.	12/14/81		
4. Implement corrective actions:			
Minor process change	01/04/82		
Major process change	03/01/82		

GENERAL INSTRUMENT

FY'82 ACTION PLANS

GROUP: MICROELECTRONICS

DIVISION: CHANDLER

DEPT/PROJECT B.2.3

DATE: November 11, 1981

KEY RESULT OBJECTIVE:

PASS PYRO INTEGRITY TEST QCI 30343; REDUCE SOFT FAILURE RELIABILITY PROBLEM.

QUANTITATIVE OBJECTIVE

TARGETED COMPLETION DATE
March 1, 1982

PRIME RESPONSIBILITY
M. Strnad/F. Hallman

TACTICAL ACTION PROGRAM:	DATE OF ACTION PLANNED	DATE OF ACTION TAKEN	STATUS/COMMENTS
1. EVALUATE PYRO DEPOSITION	COMPLETE	10/81	INDIVIDUAL RESPONSIBILITY: R. RAVINDHRAN - WAFER C L. WEI - WAFER B
2. EVALUATE PYRO PHOTO AND ETCH	11/25/81		
3. EVALUATE PYRO PHOTO	11/25/81		
4. INVESTIGATE BEST SOLUTIONS (MASKS, RESIST COAT THICKNESS, ETC.)	12/18/81		
5. IMPLEMENT CORRECTIVE ACTION			*PYRO DEPOSITION PASSES IN BOTH MODULES
MINOR PROCESS CHANGE	01/04/82		
MAJOR PROCESS CHANGE	03/01/82		

GENERAL INSTRUMENT

FY'82 ACTION PLANS

GROUP: MICROELECTRONICS

DIVISION: CHANDLER

DEPT/PROJECT: B.2.1

DATE: NOVEMBER 10, 1981

KEY RESULT OBJECTIVE:

Eliminate Exposed Gate Oxide Life Problem ("Soft" Failures).

QUANTITATIVE OBJECTIVE

TARGETED COMPLETION DATE: February 4, 1982

PRIME RESPONSIBILITY: R. C. Musa

TACTICAL ACTION PROGRAM:	DATE OF ACTION PLANNED	DATE OF ACTION TAKEN	STATUS/COMMENTS
1. Initial Implant Study.			Completed.
2. Fabricate Wafers.			Completed.
3. Package RAM's on Life.		11/7/81	Ongoing - No soft fails after 48 hours.
4. End of Life (384 hours).	11/30/81	11/23/81	Test had 14 failures, Control had 7. (27 units in each cell).
5. Second Grouping for Process Qualification and more thorough evaluation.			
Start Wafers (STIC's and RAM's).	12/1/81		Enhancement and killer implant cells in process.
Wafers Out and Probed.	12/8/81		
Onto Life Test.	12/18/81		
1000 hr. Data.	2/15/82		
Customer Samples	2/15/82		
Production Implementation.	3/1/82		

R.C. Musa

GENERAL INSTRUMENT

FY'82 ACTION PLANS

GROUP: MICROELECTRONICS

DIVISION: CHANDLER

DEPT/PROJECT: B.1.5

DATE: November 11, 1981

KEY RESULT OBJECTIVE:

Implement corrective action required for Probe, Shipping, and Kaohsiung Assembly.

QUANTITATIVE OBJECTIVE

TARGETED COMPLETION DATE: December 30, 1981

PRIME RESPONSIBILITY: C. Stockson

TACTICAL ACTION PROGRAM:	DATE OF ACTION		STATUS/COMMENTS
	PLANNED	TAKEN	
1. Eliminate all unnecessary handling of wafers after Probe.	11/18/81	11/18/81	Reduce post-Probe inspection to wafers below action yield. Currently 100% inspectien.
2. Train all Probe operators on proper handling techniques.	12/2/81	11/24 and ongoing	Completed. Using 4" wafer tweezers and Training Department is involved in training.
3. Investigate wafer boat holding trays for easier removal of wafers from boats.	12/15/81		Initial design completed and preven-out. Production quantities on order.
4. Train wafer packing operators on handling techniques and ship in Wacker containers.	11/14/81	11/8/81	Implemented Wacker containers on 11/8/81. Polyethylene bag sealer on order.
5. Implement all other recommendations of report on metal damage.	12/30/81		

GENERAL INSTRUMENT

FY'82 ACTION PLANS

GROUP: MICROELECTRONICS

DIVISION: CHANDLER

DEPT/PROJECT B.1.4

DATE: November 11, 1981

KEY RESULT OBJECTIVE:

Determine source of metal damage after wafer processing.

QUANTITATIVE OBJECTIVE

TARGETED COMPLETION DATE
December 1, 1981

PRIME RESPONSIBILITY
C. Stockson

TACTICAL ACTION PROGRAM:	DATE OF ACTION PLANNED	DATE OF ACTION TAKEN	STATUS/COMMENTS
1. Inspect wafers before and after Probe.	11/08/81	11/08 and ongoing	Data indicated that actual metal damage on uninked die is less than 2%. However, contaminants on die induce metal damage during the shipping of the wafers.
2. Inspect wafers after packing.	11/08/81	11/08 and ongoing	Wafer damage is 10% to 12% after post packing inspection.
3. Investigate Assembly wafer handling in Kaohsiung.	12/01/81	11/24/81	G. Pickthall is in Kaohsiung and is doing a survey Assembly handling. Kaohsiung damage is 1 - 2%.
4. Issue report on results and recommendations.	12/01/81		

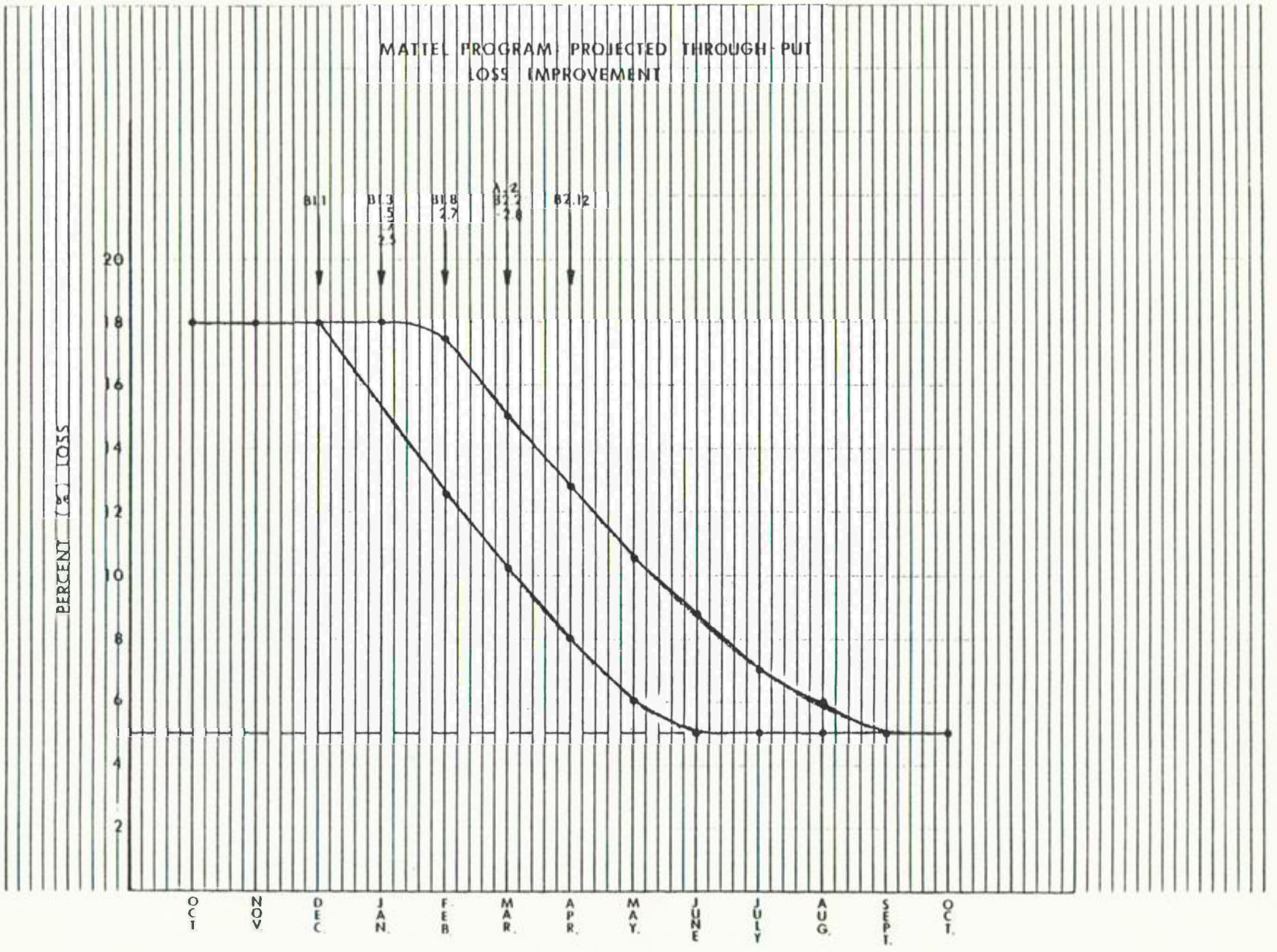
Mattel Program - Effects on Process Through-Put Losses (Percentage Points) Forecasted For Changes Implemented Within General Instrument.

	Nov.	Dec.	Jan.	Feb.	Mar.	Apr.	May	June	July	August	September	Total
A. 1.x (C.P.S./Testing)						1/1	1/1	1/0.5	1/0.5	/0.5	/0.5	4
B. 1.1 - 1.7 (Hard Failures)					3/1	/0.5	/0.5	/0.5	/0.5			3
B. 1.8 (Hard Failures)				0.5/0.5	1/0.5	0.25/0.25	0/25/0.25	/0.25	/0.25			2
B. 2.x					1/1	1/0.5	1/0.5	1/0.5	/0.5	/0.5	/0.5	4
Through-Put Losses	18/18	18/18	18/18	17.5/17.5	12.5/15.0	10.25/12.75	8/10.5	6/8.75	5/7	5/6	5/5	

NOTE: X/Y X = Forecasted (Optimistic?) Number

Y = Program Manager Judged Number

R. P. Jones
11/30/81


MATTEL PROGRAM: PROJECTED THROUGH-PUT
LOSS IMPROVEMENT
PERCENT (%) LOSS
20
18
16
14
12
10
8
6
4
2
B1.1
B1.3
B1.8
2.7
B2.12
OCT
NOV
DEC
JAN.
FEB.
MAR.
APR.
MAY.
JUNE
JULY
AUG.
SEPT.
OCT.